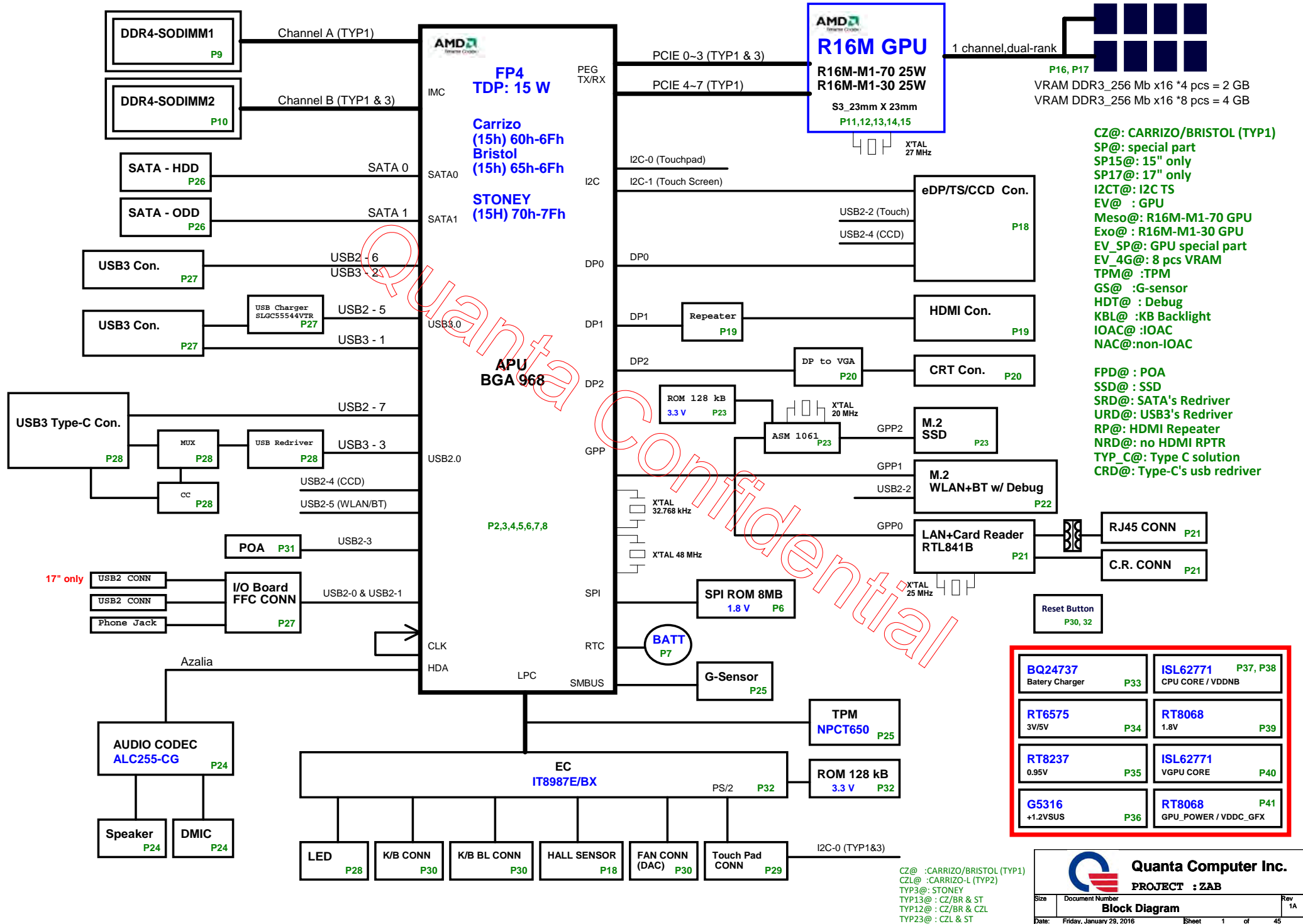


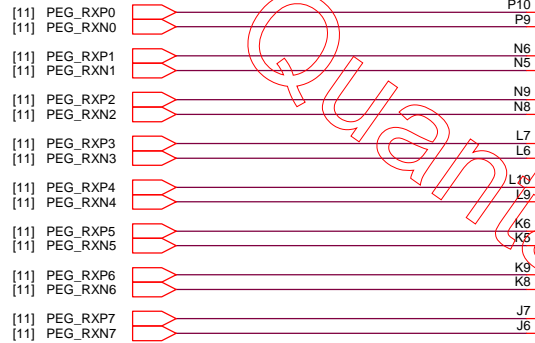
ZAB/ZAB A,B/ZYJA BLOCK DIAGRAM



1.05V VDDP only for CZ with DDR-2133 memory
If running DDR-1866 or slower memory,
Platform VDDP should be set to 0.95V
TYP13: (196R_CS11962FB00)
TYP1: (1.69K_CS21692FB01)
CZL: (1.69K_CS21692FB01)

X8: TYP1 (GEN3)

X4: TYP3 (GEN3)

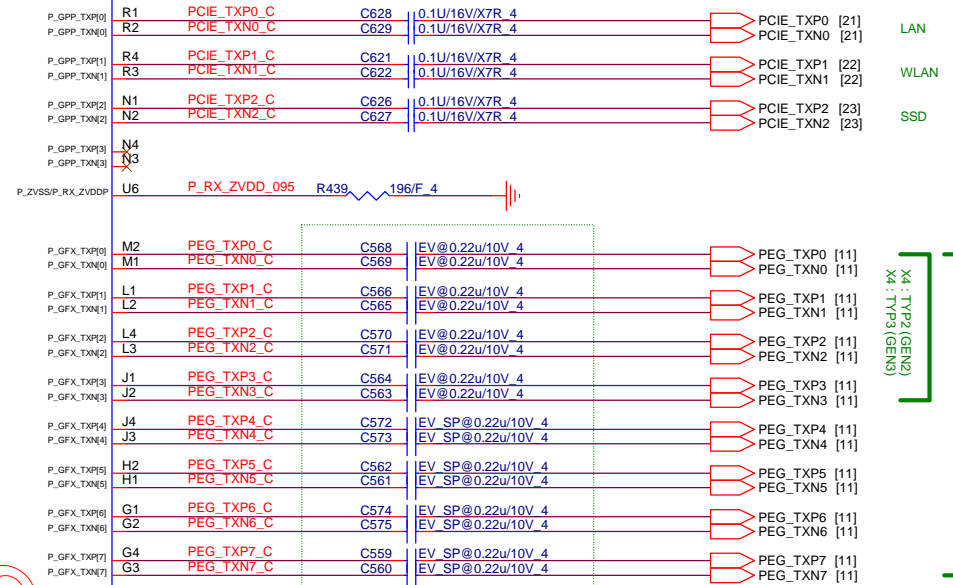


FP4 REV 043

SPB/FP4

AC-coupling capacitor(depend on GenX, not TYPE)
TYP1&3:(220nF)CH4222K9B04: Only Gen3 and Both of Gen2&3
TYP2 : (100nF)CH4103K1B08: Only Gen2

TYP2 no Gen3



AC-coupling capacitor(depend on GenX, not TYPE)
TYP1&3:(220nF)CH4222K9B04: Only Gen3 and Both of Gen2&3
TYP2 : (100nF)CH4103K1B08: Only Gen2



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PROJECT : ZAB

Size	Document Number	Rev
	FP4 PCIe I/F (1/7)	1A
Date:	Monday, February 15, 2016	Sheet 2 of 45

U31A

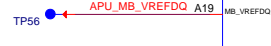


+1.2VSUS

```

M_B_DQ[0..63]  [10]

```

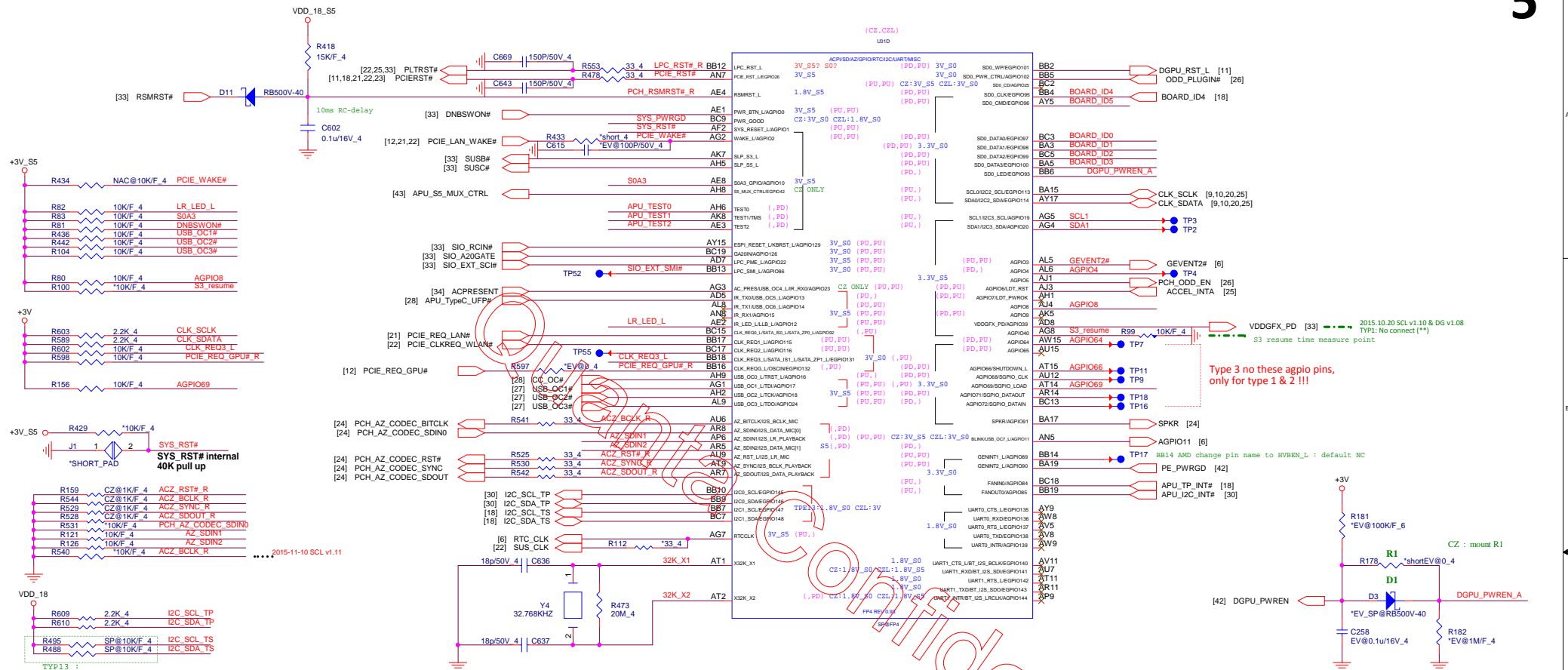


SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

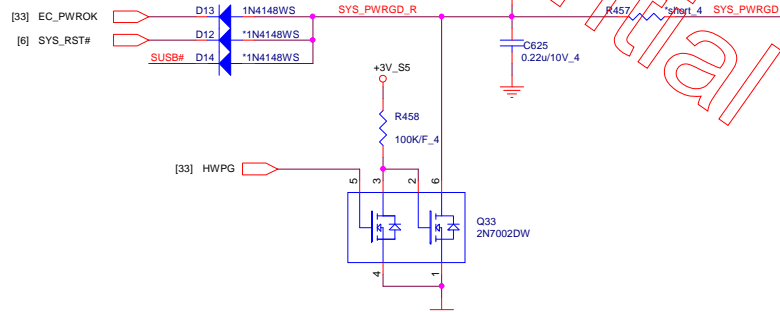
HDT(Hardware Debug Tool) Connector

The diagram illustrates the electrical connections for the HDT (Hardware Debug Tool) Connector. Key components and connections include:

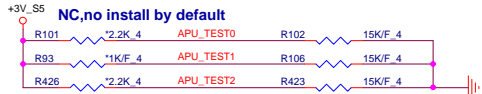
- U33 (HDT@SN74LVC2G07DCKR):** A hex inverter buffer used for signal conditioning. It connects **APU_RST#** (pin 1A) to **APU_RST_L_BUF** (pin 1Y) and **APU_PWROK_D** (pin 2A) to **APU_PWROK_BUF** (pin 2Y). Its VCC (pin 6) is connected to **VDD_18**, and its GND (pin 5) is connected to ground.
- Connector CN7:** Labeled "PLACE HDT+ HEADER ON TOP", it provides the interface between the HDT and the APU.
 - Pin 1:** CPU_VDDIO
 - Pin 2:** CPU_TCK
 - Pin 3:** GND
 - Pin 4:** CPU_TMS
 - Pin 5:** GND
 - Pin 6:** HDT_APU_TDI
 - Pin 7:** GND
 - Pin 8:** CPU_TDO
 - Pin 9:** APU_TDO
 - Pin 10:** APU_PWROK_BUF
 - Pin 11:** CPU_PWROK_BUF
 - Pin 12:** APU_RST_L_BUF
 - Pin 13:** CPU_RST_L_BUF
 - Pin 14:** CPU_DBRDY
 - Pin 15:** CPU_DBRDY2
 - Pin 16:** HDT_DREQ#
 - Pin 17:** CPU_DBRDY1
 - Pin 18:** CPU_DREQ_
 - Pin 19:** GND
 - Pin 20:** CPU_FLLTEST#
 - Pin 21:** APU_TEST19
 - Pin 22:** APU_TEST18
- Power and Grounding:**
 - VDD_18:** The primary power supply for the HDT, connected to pins 6 and 19 of U33, and to various decoupling capacitors (C218, C674, C675, C719).
 - Grounding:** Multiple GND pins on the HDT and APU are connected to a common ground plane.
- Signal Conditioning:**
 - APU_RST#:** An active-low reset signal from the APU, buffered by U33 to **APU_RST_L_BUF**.
 - APU_PWROK_D:** A debug signal from the APU, buffered by U33 to **APU_PWROK_BUF**.
 - APU_TDO:** A test data output from the APU, connected to pin 9 of CN7.
 - APU_TEST19/18:** Test signals from the APU connected to pins 21 and 22 of CN7.
- Decoupling and Protection:**
 - R160, R161, R162, R163, R164:** Resistors used for signal termination and protection on the HDT header.
 - R562, R563, R564, R565, R566, R567, R568, R569:** Resistors used for signal termination and protection on the APU header.
 - C218, C674, C675, C719:** Decoupling capacitors for power and signal lines.



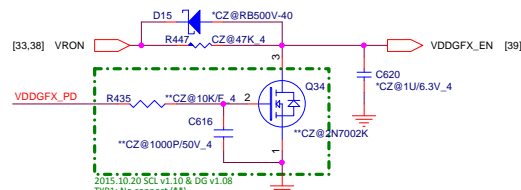
SYS PWGRD



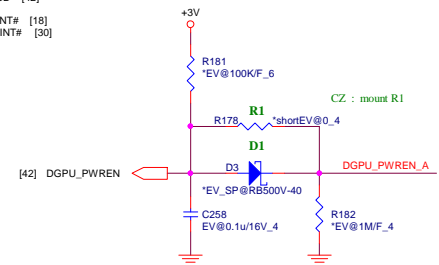
Test mode setting (Follow AMD's suggestion)



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

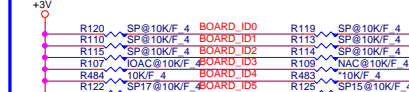


Type 3 no these agpio pins, only for type 1 & 2 !!!



BOARD ID

ZYV
BOARD_ID4 Depend on cable => always PU, PD DNI
Touch cable PIN2 => NC
non-Touch cable PIN2 => GND



GPIO	High	Low
BOARD_ID0	dTPM	iTPM
BOARD_ID1	dGPU	UMA
BOARD_ID2	non-G sensor	G sensor
BOARD_ID3	IOAC	non-IOAC
BOARD_ID4	Touch	non-Touch
BOARD_ID5	17"	15"

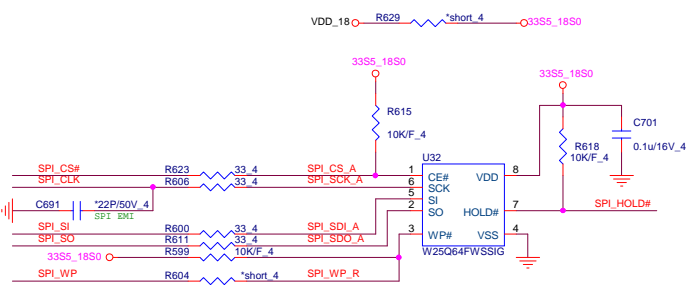
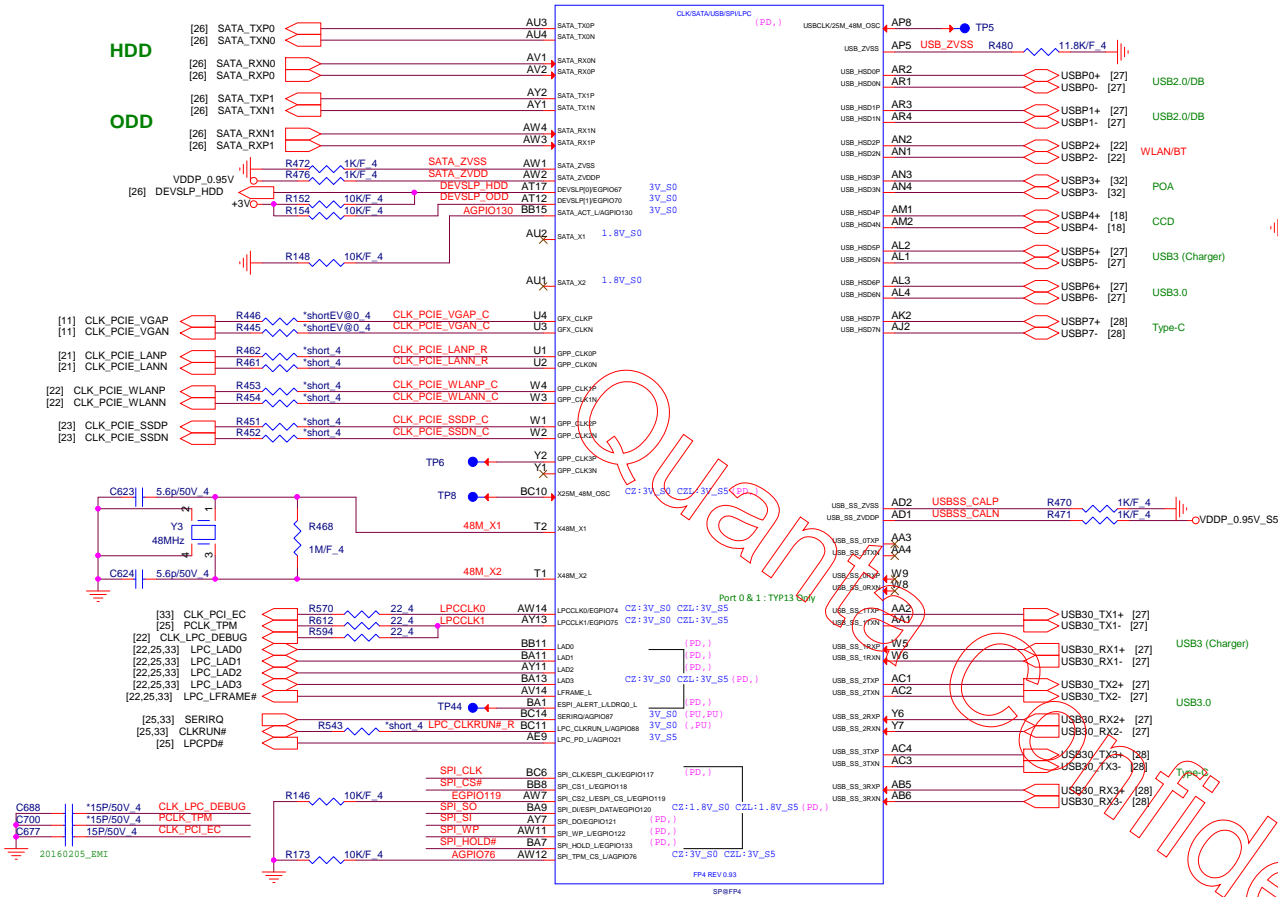


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PROJECT : ZAB

HDD

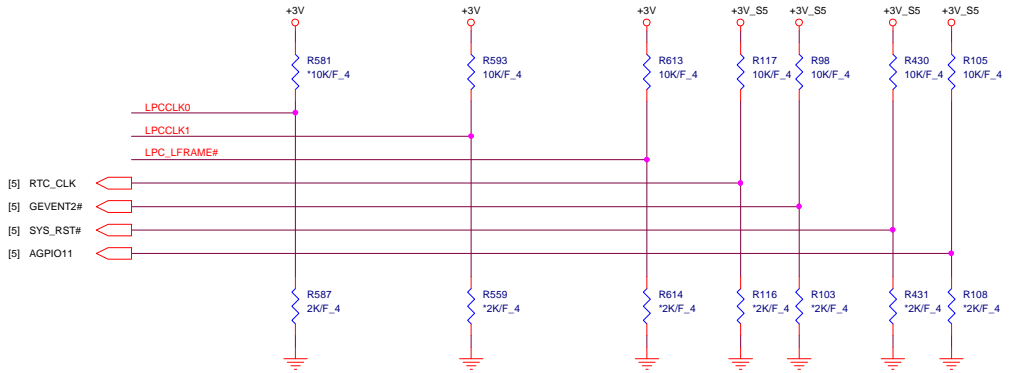
ODD



SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
TYP13 1.8V	WND	8M	AKE5EZNO00	W25Q64FWSSIG
	GGD	8M	AKE5EG-0Q00	GD25LQ64CSIGR
	EON	8M		

STRAPS PINS



	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2# (AGPIO3)	SYS_RST#	AGPIO11(BLINK)
PU	BOOT Fail Timer ENABLE	Internal CLKGEN	SPI ROM	Coin battery is on board.	1.8V SPI ROM Enhanced Reset logic	normal reset mode	LDT_RST#/LDT_PWRGD output to APU
PD	BOOT Fail Timer DISABLE	External CLKGEN	LPC ROM	Coin battery isn't on board.	3.3V SPI ROM Traditional Reset logic	short reset mode	LDT_RST#/LDT_PWRGD output to Pads

22 uF * 8
0.22 uF * 6
180 pF * 1

10 uF * 4
0.22 uF * 6
180 pF * 1

22 uF * 4
0.22 uF * 8
180 pF * 1

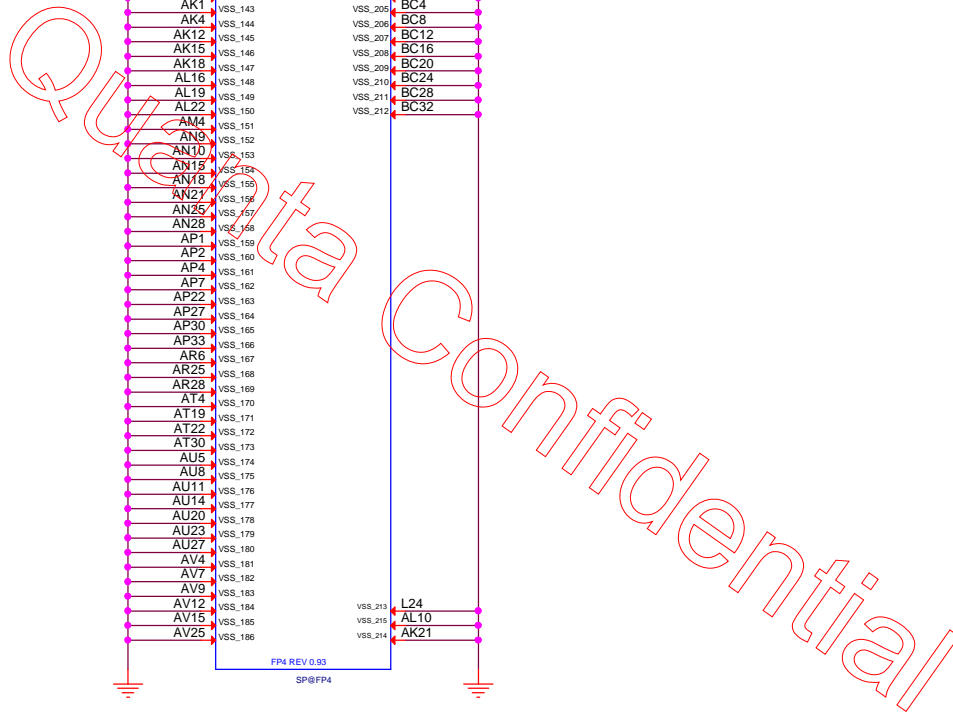
22 uF * 9
0.22 uF * 8
180 pF * 1

22 uF * 9
0.22 uF * 9
180 pF * 1

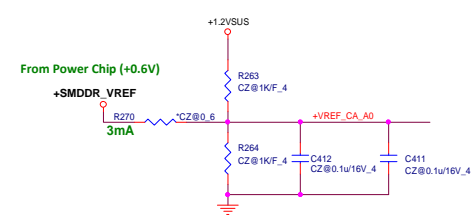
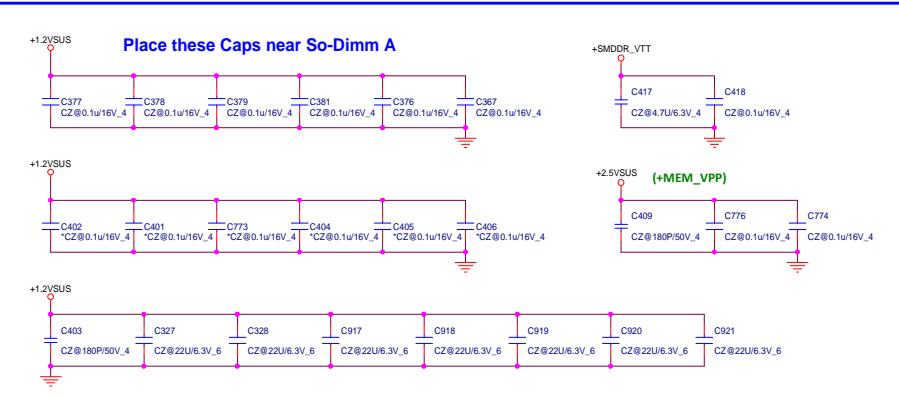
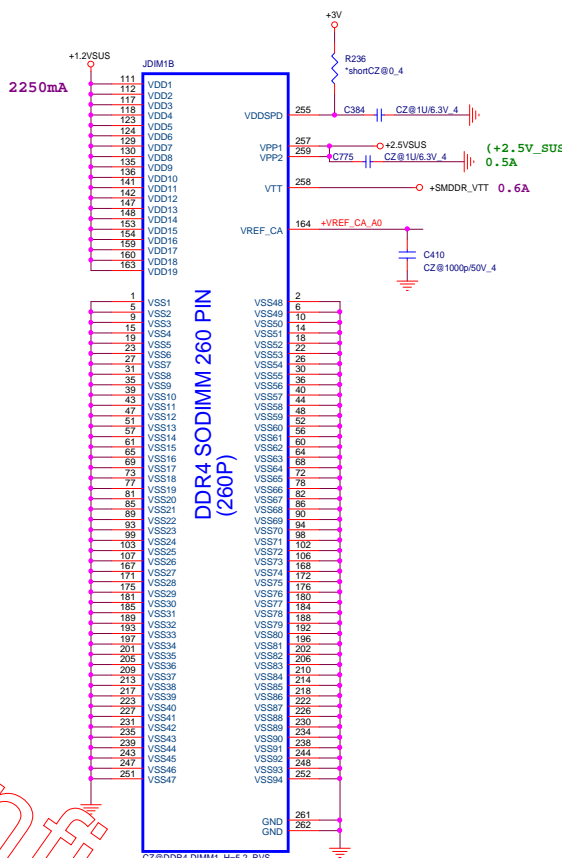
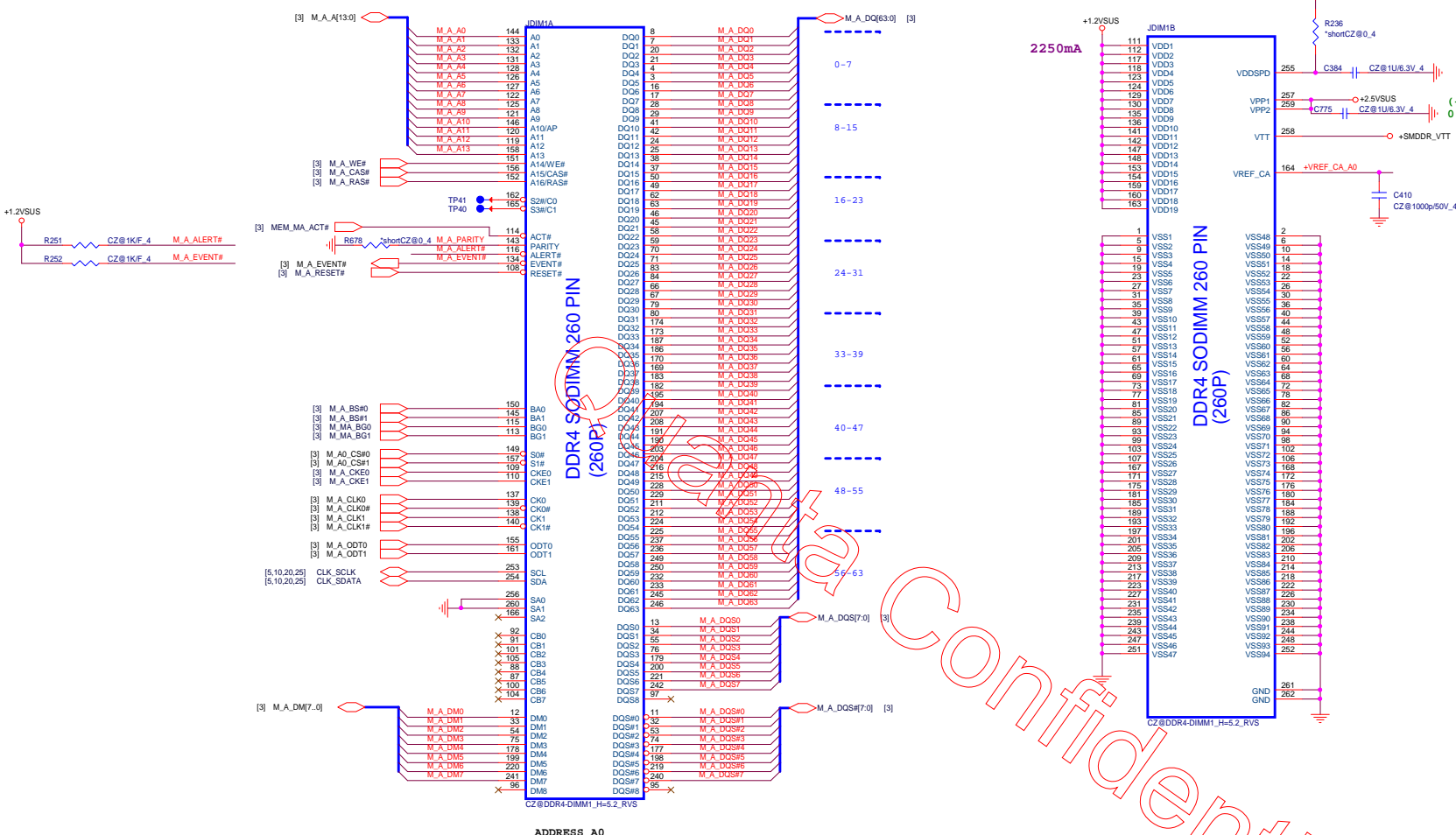
RTC (RTC)

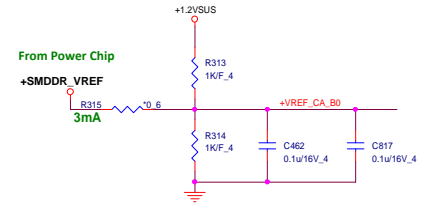
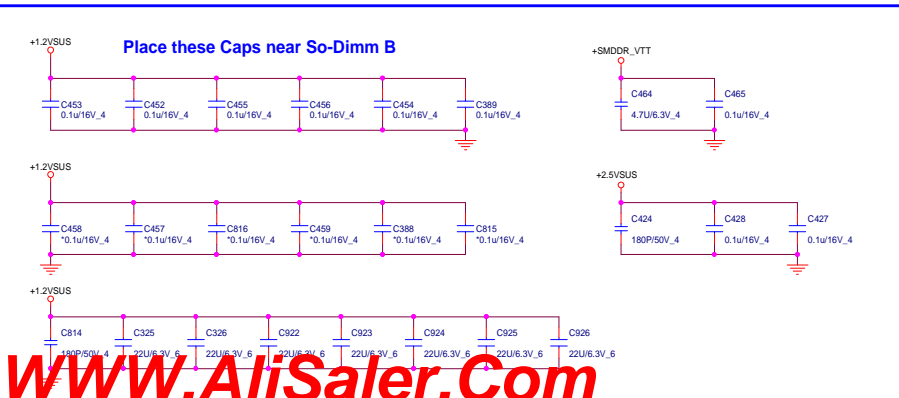
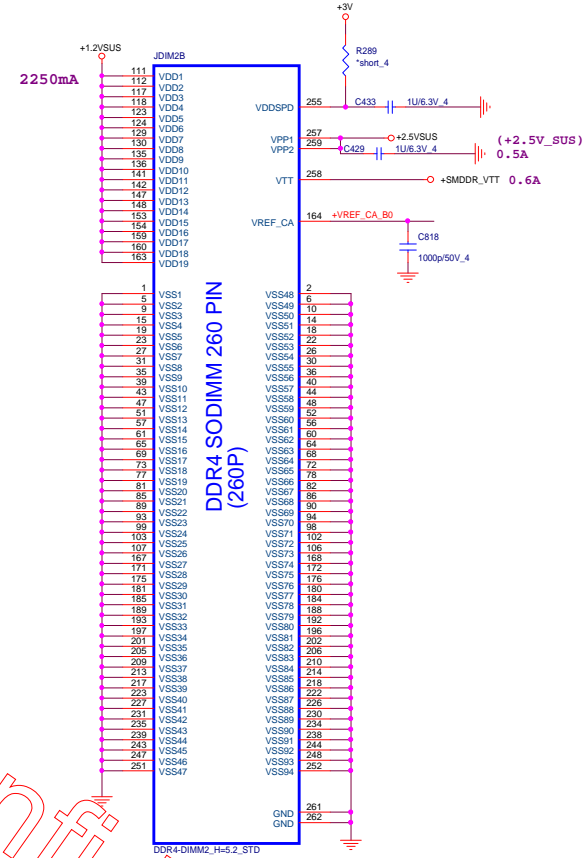
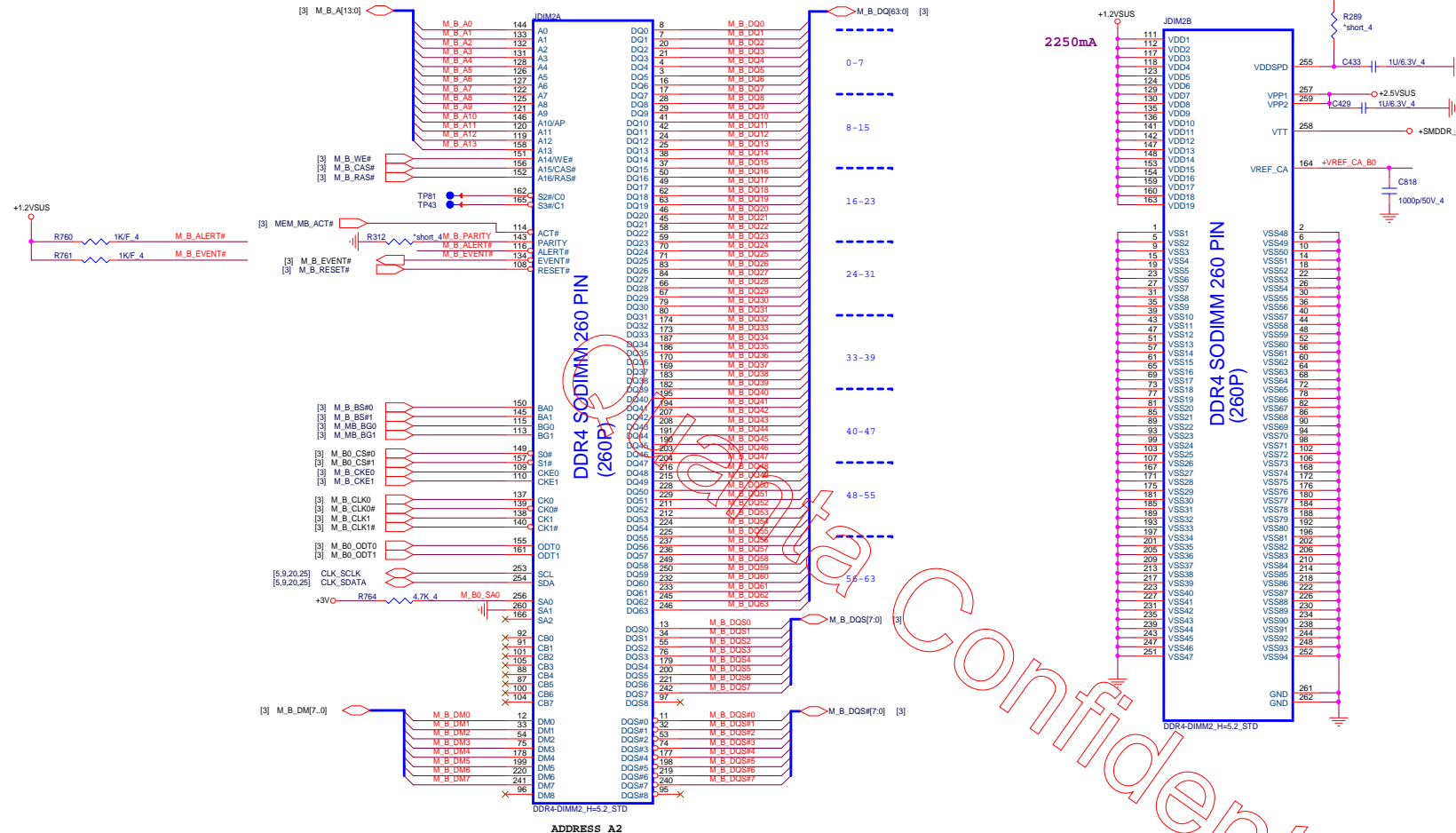
For EC reset RTC

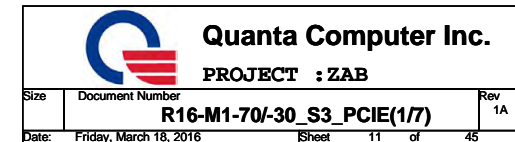
RTC CR2032 Coin Battery
DBV: AHL03003057
VDE: AHL03003003
JHT: AHL03003035



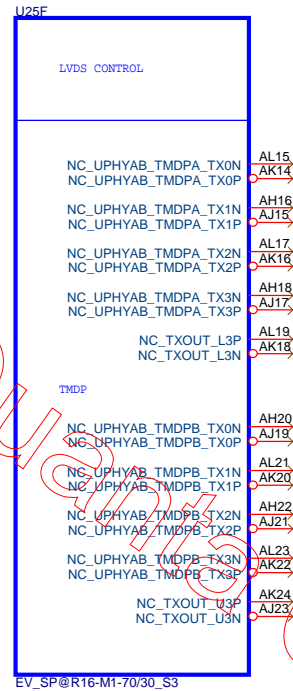
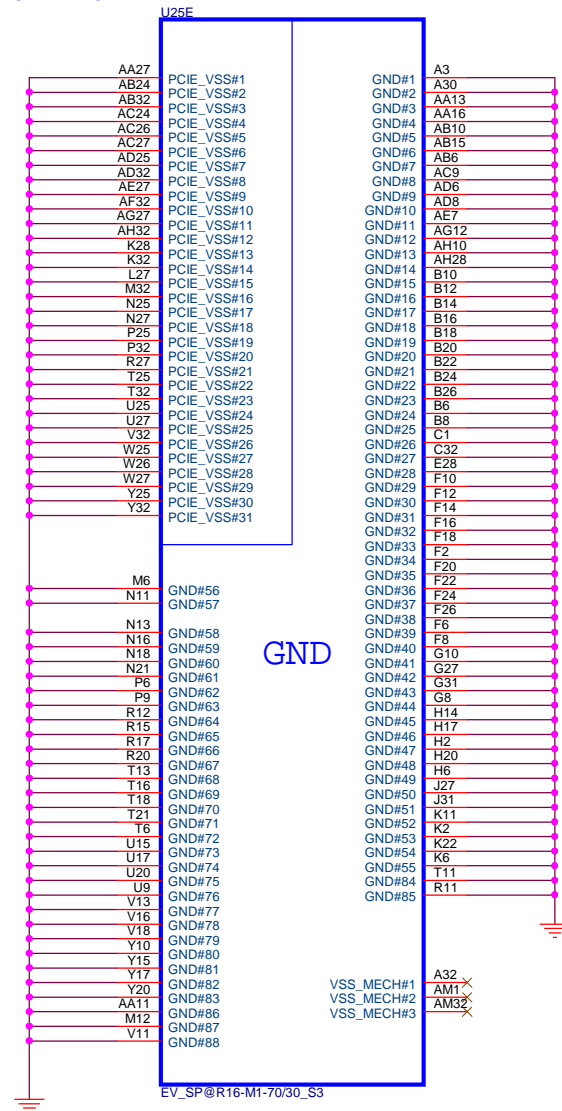
SODIMM (SDM)







(VGA)

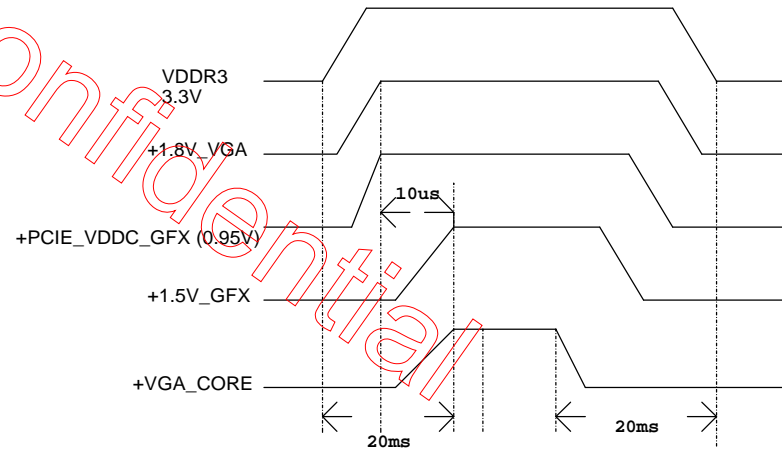


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.

It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

For power down, reversing the ramp-up sequence is recommended.

Power Up/Down Sequence



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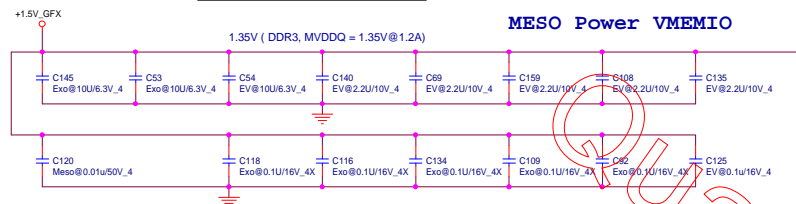
PROJECT : ZAB

Size	Document Number	Rev
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Date: Friday, March 18, 2016 Sheet 13 of 45

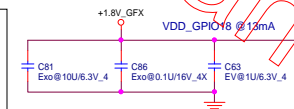
VDDR1	
EXO	MESO
10u X3	10u X1
2.2u X5	2.2u X5
0.1u X6	0.1u X1
	0.01u X1

PCIE_PVDD	
EXO	MESO
10u X1	10u X1
1u X1	1u X1
0.1u X1	
0.01u X1	



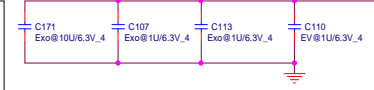
Meso Power VDD_GPI018

VDD_CT	
EXO	MESO
bead 120 X1	1u X1
10u X1	
0.1u X1	

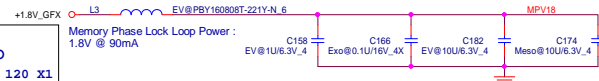


Meso Power VDD_GPI033

VDDR3	
EXO	MESO
bead 120 X1	1u X1
10u X1	
1u X3	



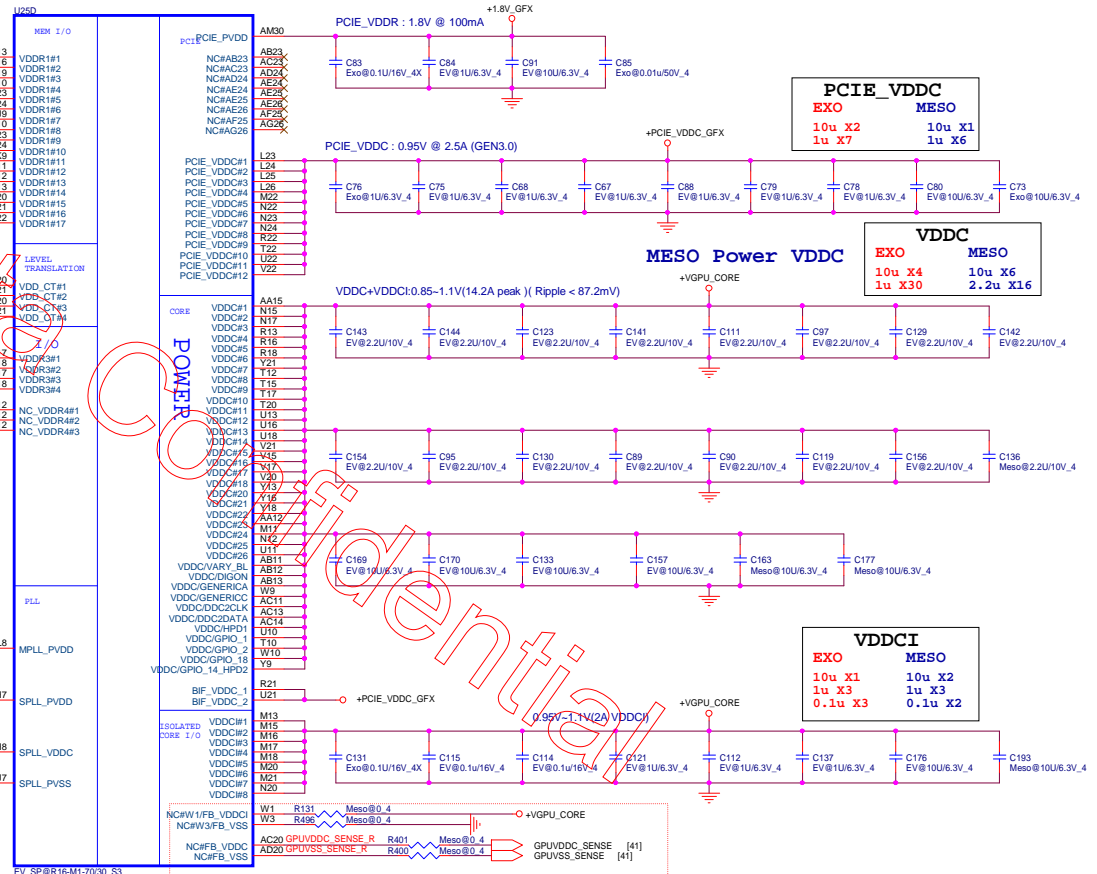
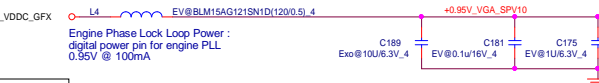
MPLL_PVDD	
EXO	MESO
bead 220 X1	bead 220 X1
10u X1	10u X2
1u X1	1u X1
0.1u X1	

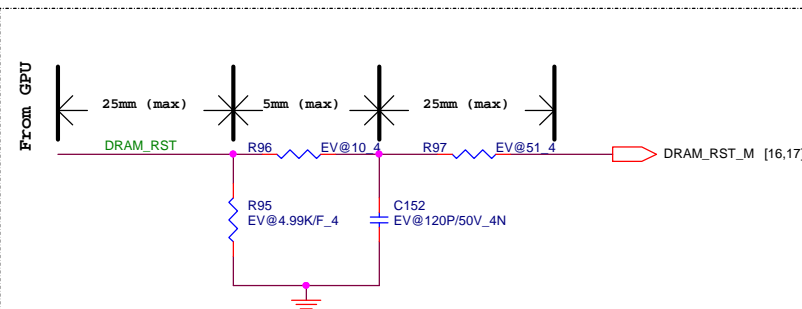
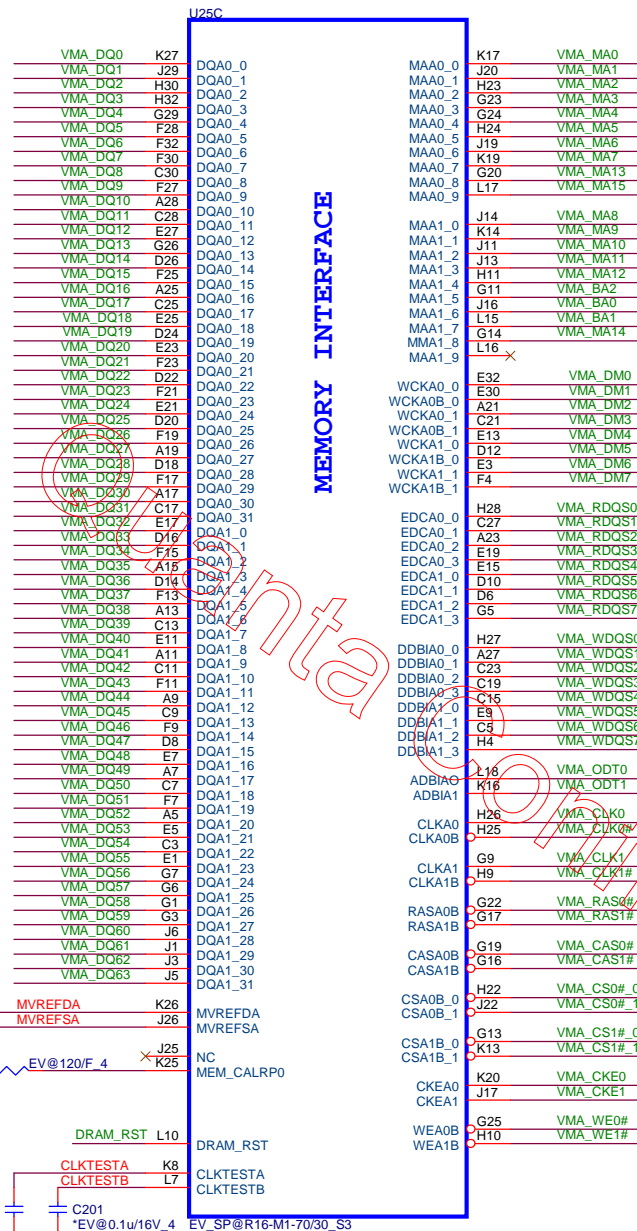
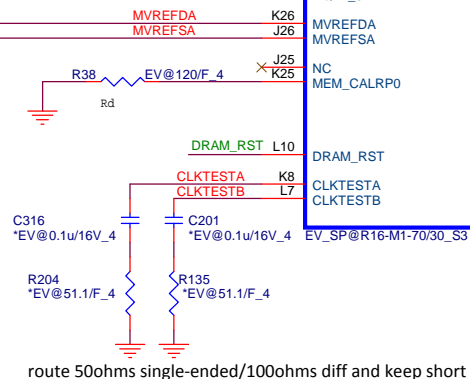
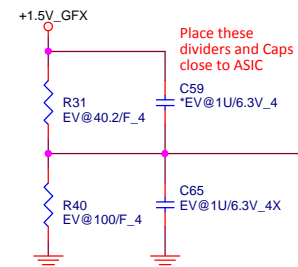


SPLL_PVDD	
EXO	MESO
bead 120 X1	bead 120 X1
10u X1	1u X1
1u X1	10u X1
0.1u X1	



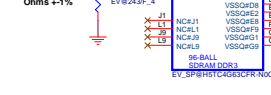
SPLL_VDDC	
EXO	MESO
bead 120 X1	bead 120 X1
10u X1	1u X1
1u X1	0.1u X1
0.1u X1	

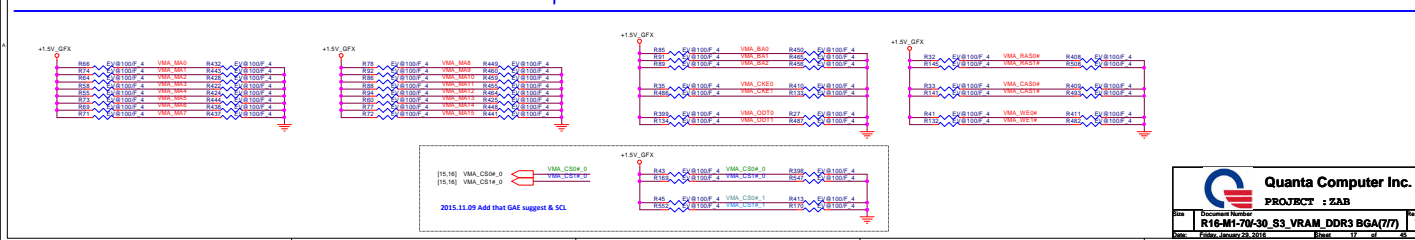




Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.





OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



Add it when using HDMI level shifter



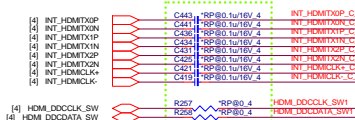
Equalizer settings

Inputs		Equalization for 3 Gears
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

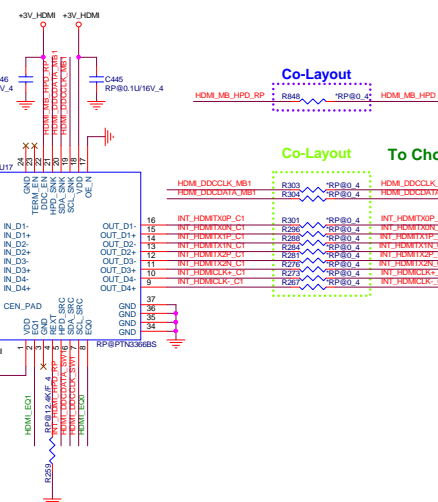


From APU

Co-Layout



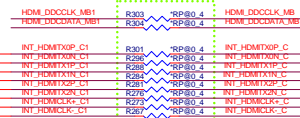
Co-Layout



Co-Layout

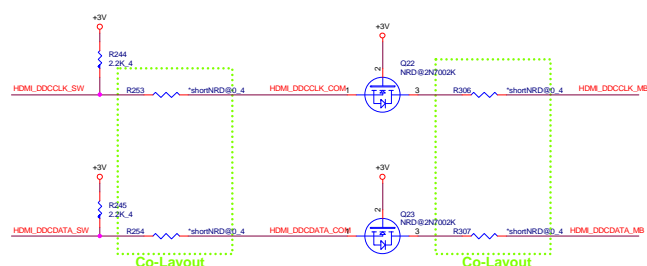
Co-Layout

To Choke



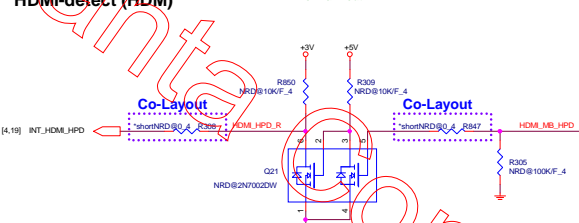
HDMI DDC (HDM)

Normal Rout



HDMI-detect (HDM)

Normal Rout

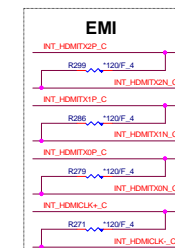
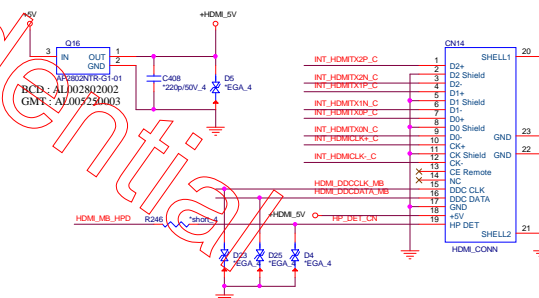
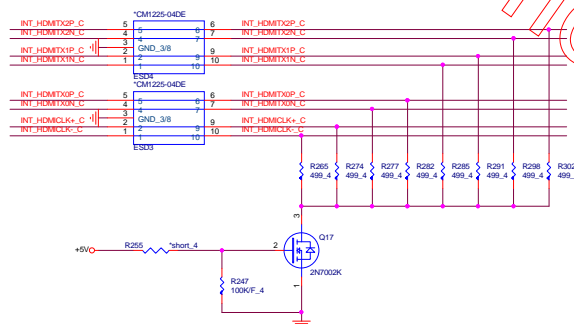
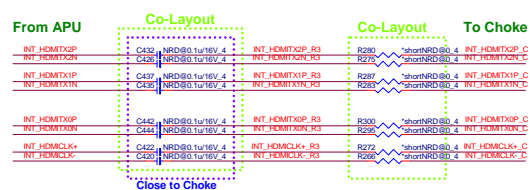


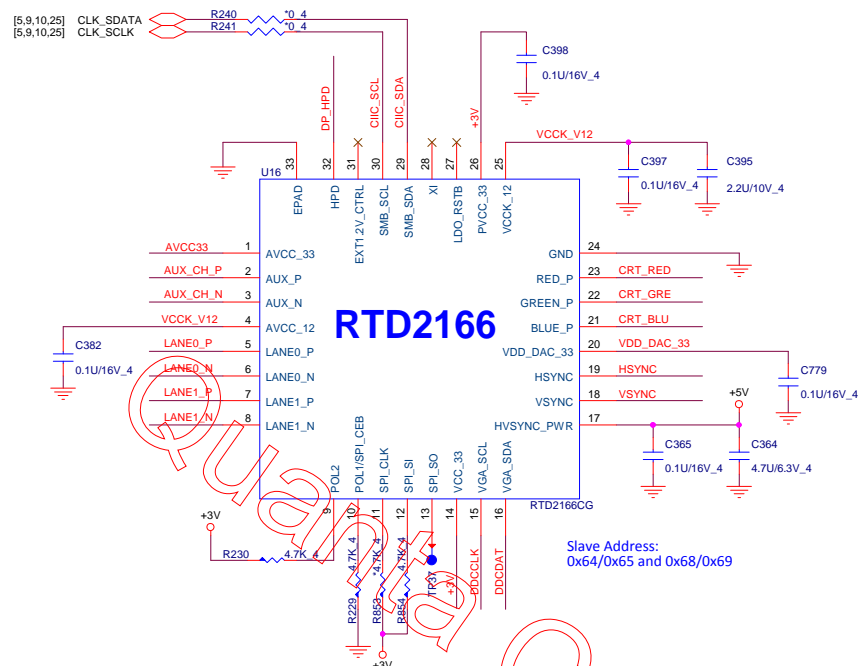
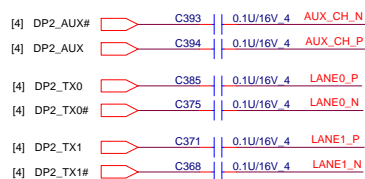
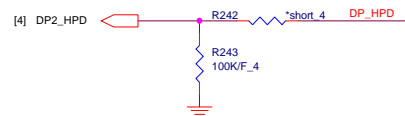
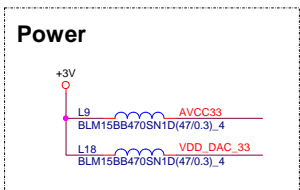
****Share with normal rout**



HDMI(HDM)

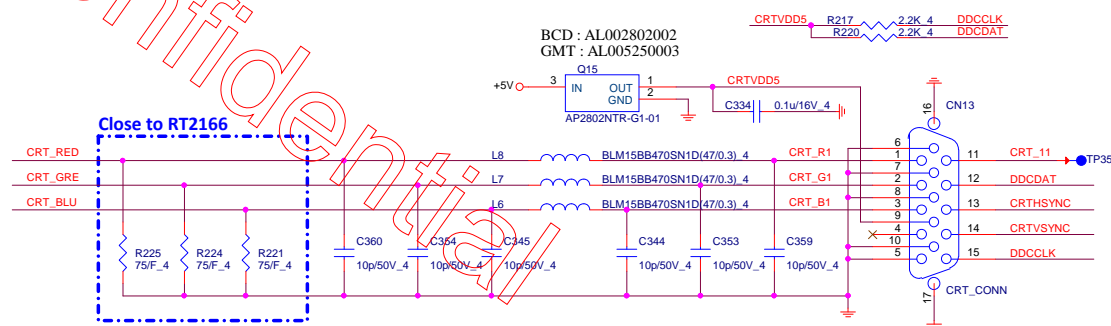
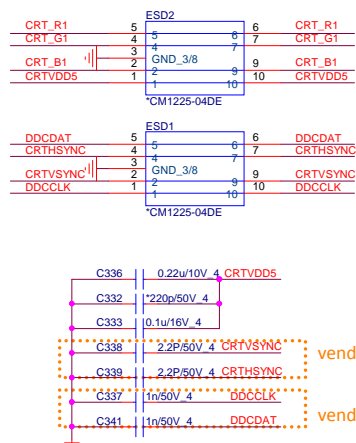
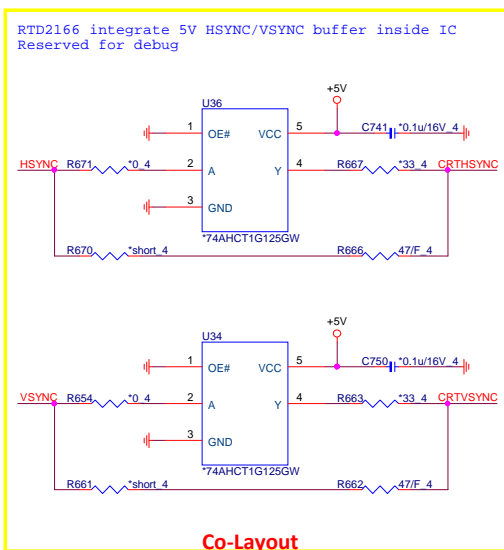
Final Route

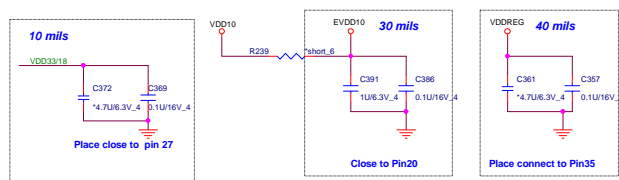
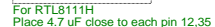




Note:

- 1- Caps should be placed close to chip
- 2- Pin 9's Cap should be X5R material
- 3- R,G,B's R should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.





All termination trace > 30 mils

U35

1 TC1T MCT1 24 LAN_MCT0

3 TD1+ MX1+ 25 LAN_MX0

4 TC2T MCT2 21 LAN_MCT1

5 TD1- MX1- 20 LAN_MX1

6 TC2T MCT2 19 LAN_MCT2

7 TD2+ MX2+ 18 LAN_MX2

8 TC3T MCT3 17 LAN_MX3

9 TD3+ MX3+ 16 LAN_MX3

10 TC4T MCT4 14 LAN_MCT4

11 TD4+ MX4+ 13 LAN_MX4

12 TD4- MX4- 13 LAN_MX4

TRANSFORMER

C331
0.01u50V/X7R_4

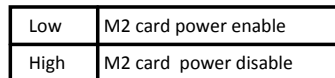
TERA99

C714
100p3KV_180

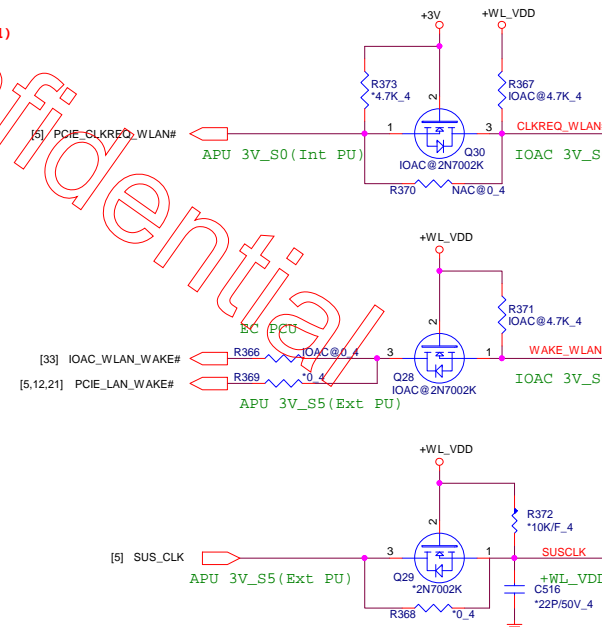
Pinout diagram for LAN connector CN10. The diagram shows a 10-pin connector with pins 1 through 8 labeled LAN_MX0+ through LAN_MX3-. Pins 9 and 10 are labeled 10 and 9 respectively. The connector is labeled CN10 and CONN RJ45 SINK. The internal wiring shows a cross-over pattern: LAN_MX0+ to 12, LAN_MX0- to 11, LAN_MX1+ to 1, LAN_MX1- to 2, LAN_MX2+ to 4, LAN_MX2- to 5, LAN_MX3+ to 7, LAN_MX3- to 8, 10 to 9, and 9 to 10.

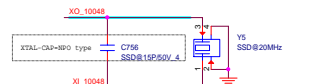
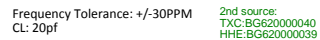
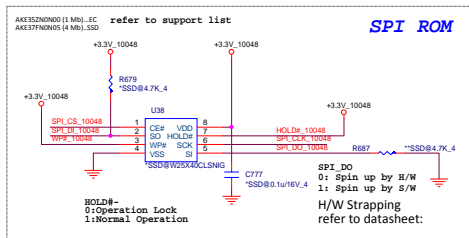
[illegible]

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMK	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS
SP8	SD CD#	



The schematic diagram illustrates the WLAN power supply circuit. It features a +1.5V_SVS input connected to a network of components. A capacitor C8 (0.1u/16V_4) is connected to the input. The circuit includes an inductor Q2 (A03413) and resistors R5 (10K/F_4) and R6 (100K/F_4). The output is labeled 3+3V_WLAN. Annotations specify IOAC values for various components: C8 at 0.1u/16V_4, R6 at 100K/F_4, R5 at 10K/F_4, and C10 at 1000p/50V_4.

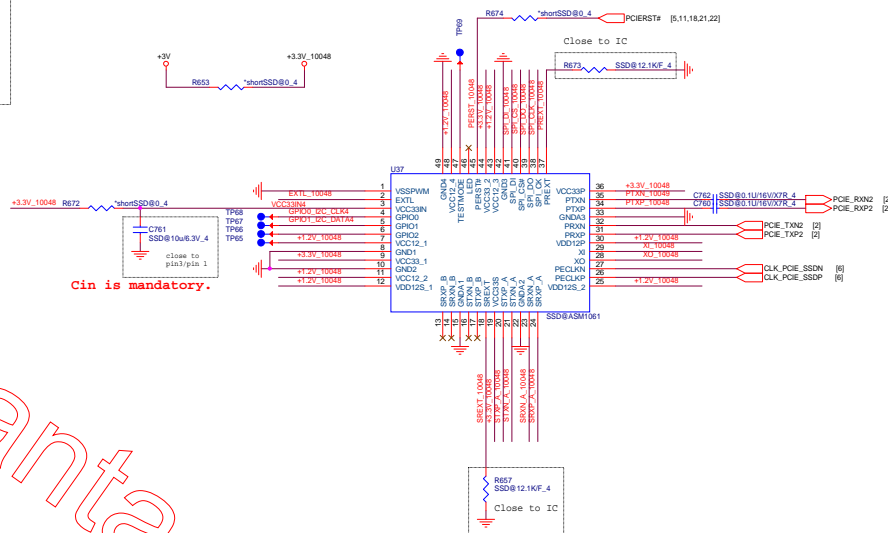




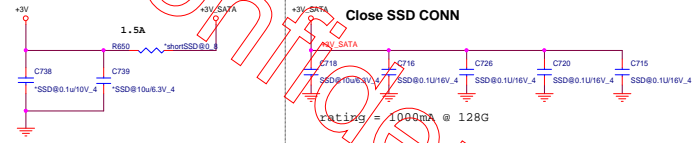
XI & XO follow differential layout rule for Min jitter

Close to ASM1061

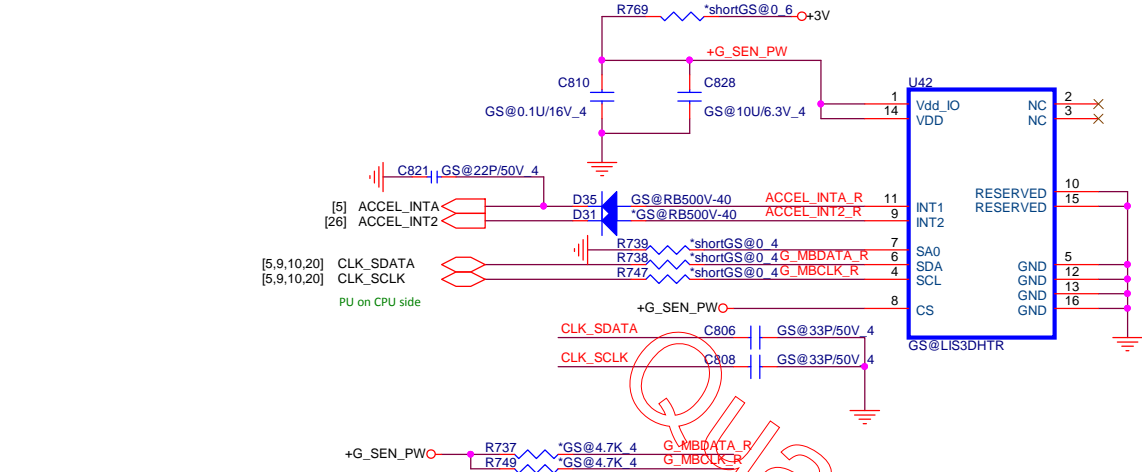
Cin is mandatory.



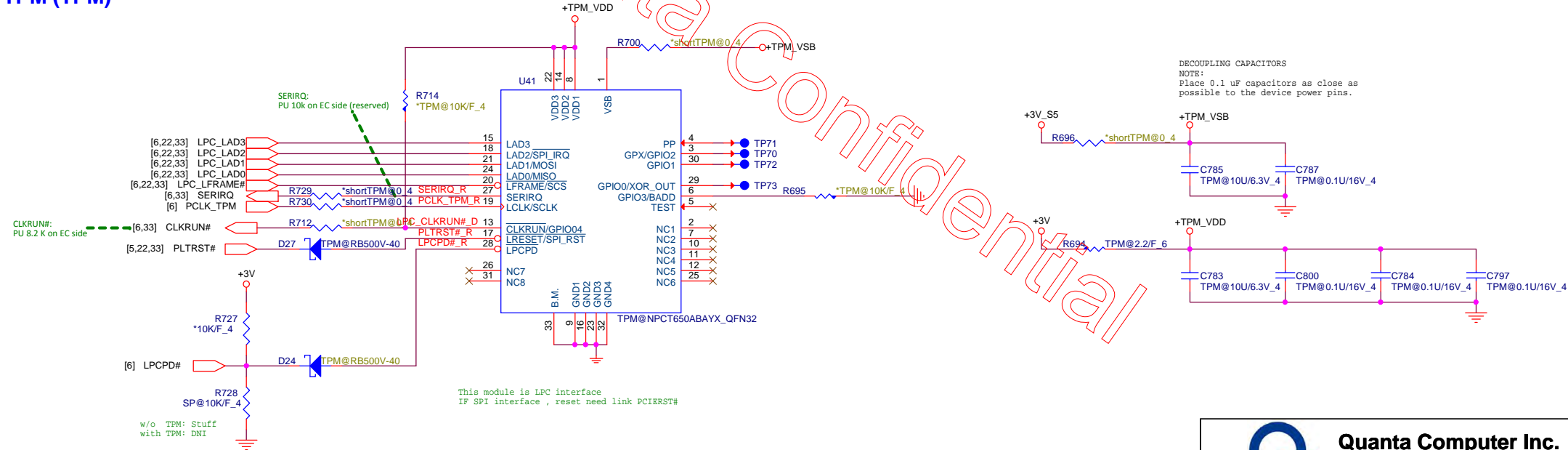
6/25 Add R580/R581 by Kingston SSD.



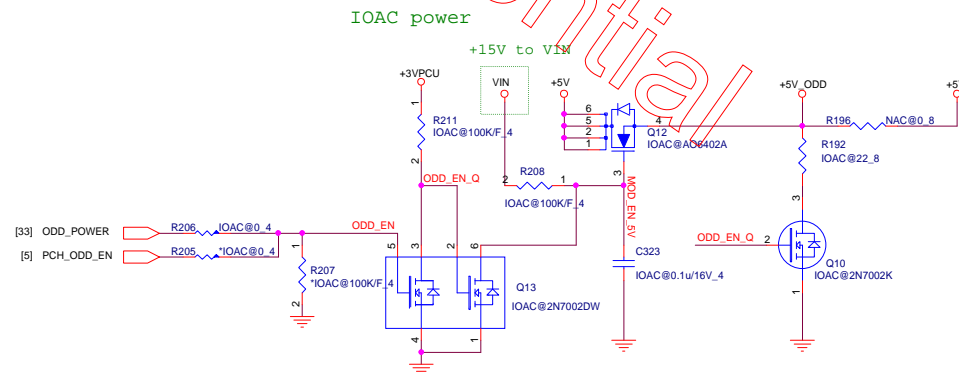
pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated.
10	DAS#	Device Activity Signal
21	WGN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP sleep signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal is: SSD enter sleep model. Device Sleep Signal:: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MPG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MPG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IPDET	This pin connect to ground

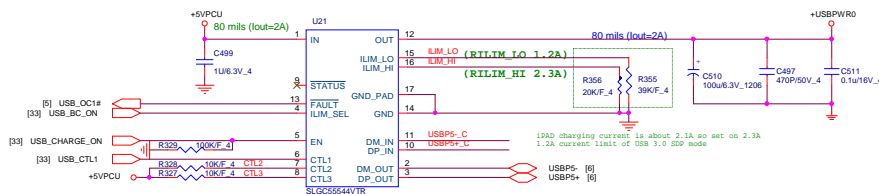


TPM (TPM)



26





GMT:AL003703000(G3703)_X
TI:AL002544001(TPS2544)
Silerqy:AL055544000(SLGC55544VTR)

	CTL1	CTL2	CTL3	ILIM_SEL
SDP	1	1	1	0
CDP	1	1	1	1
DCP	0	1	1	X

RTIM IO is optional and the RTIM IO pin may be left unconnected if the following conditions are met:

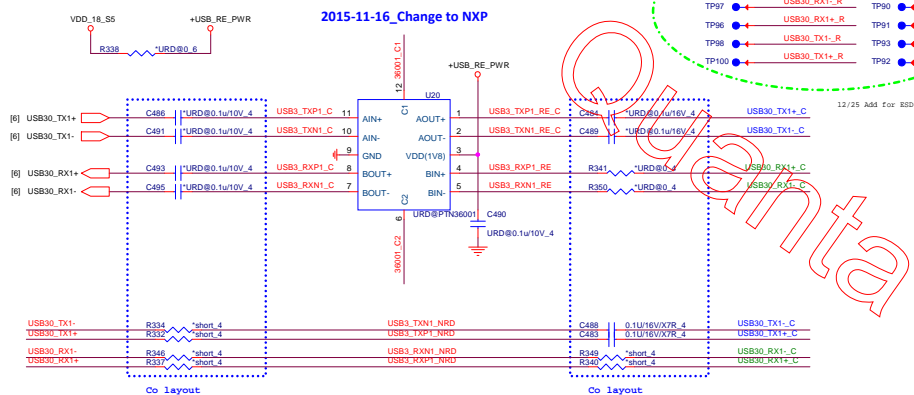
- RILIM_LO is optional and the RILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
 2. Load Detection - Port Power Management is not used
 3. Mouse / Keyboard wake function is not used
- If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate

$$\text{IOS_typ(mA)} = 50,250 / \{\text{RILIM_XX(K}\Omega\text{)} + 0.1\}$$

USB 3.0 redriver (UB3)



2015-11-16 Change to NXP

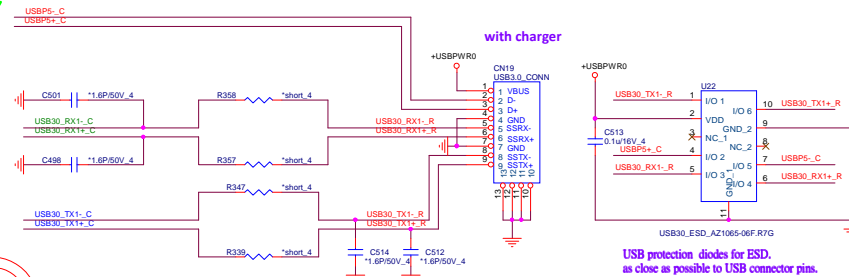
Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ	DE	OS
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

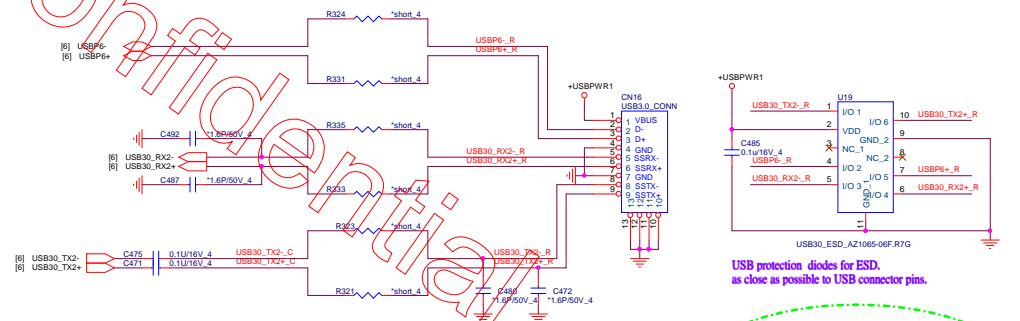
Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ ⁽¹⁾	DE ⁽²⁾	OS ⁽³⁾
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

USB 3.0 Connector (UB3)

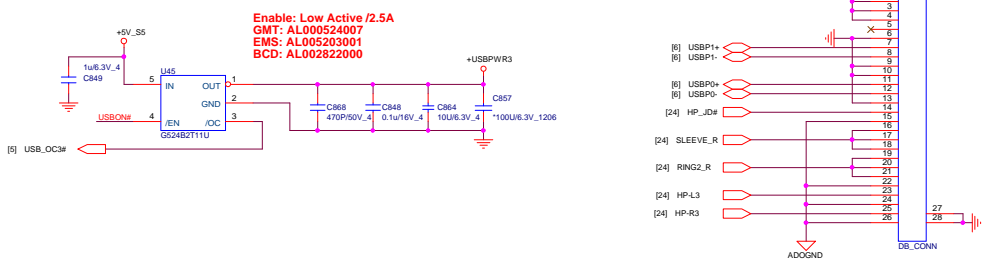


USB protection diodes for ESD,
as close as possible to USB connector pins.



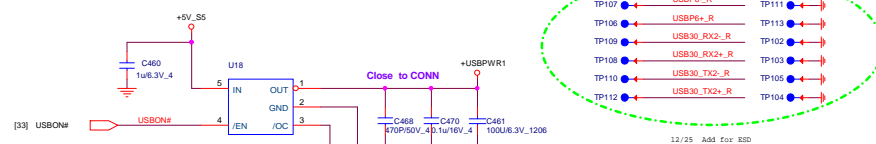
USB protection diodes for ESD,
as close as possible to USB connector pins.

DB
USB2.0 (UB2)



Enable: Low Active /2.5A
GMT: AL000524007
EMS: AL005203001
BCD: AL002822000

Enable: Low Active /2.5A
GMT:AL000524007
EMS:AL005203001
BCD:AL002822000



[illegible]

Figure 10 shows the pin connections for the CBTL02043A-QSD. The diagram illustrates two circuit boards. The top board is a 16-pin DIP package with pins 1-16 connected to various components: +V5_V5, R180, short to TP_C8@0_E, +MUX_PWR, C867, C845, C862, C851, and TP_C8@1u16V. The bottom board is a 20-pin DIP package with pins 1-20 connected to: +MUX_PWR, VDD001, VDD06, VDD10, USB3_TXP3_B0+, USB3_TXN3_B0+, USB3_RXP3_B1+, USB3_RXN3_B1+, USB3_TXP3_C0+, USB3_RXP3_C0-, USB3_TXP3_C1+, USB3_RXP3_C1-, VSS005, VSS011, VSS020, and TAB. A table at the bottom defines the pin functions for the CBTL02043ABQ_SEL pin: Low (Port A to Port B), Hi (Port A to Port C), and Normal operation (Active-low chip enable).

Pin	Function
1	+V5_V5
2	R180
3	short to TP_C8@0_E
4	+MUX_PWR
5	C867
6	C845
7	C862
8	C851
9	TP_C8@1u16V
10	TP_C8@1u16V
11	TP_C8@1u16V
12	TP_C8@1u16V
13	TP_C8@1u16V
14	TP_C8@1u16V
15	TP_C8@1u16V
16	TP_C8@1u16V
17	TP_C8@1u16V
18	TP_C8@1u16V
19	TP_C8@1u16V
20	TP_C8@1u16V

From CC Ctrl

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_SEL

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_QSD

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_QSD

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_QSD

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_QSD

Pin	Function
1	+MUX_PWR
2	VDD001
3	VDD06
4	VDD10
5	USB3_TXP3_B0+
6	USB3_TXN3_B0+
7	USB3_RXP3_B1+
8	USB3_RXN3_B1+
9	USB3_TXP3_C0+
10	USB3_RXP3_C0-
11	USB3_TXP3_C1+
12	USB3_RXP3_C1-
13	VSS005
14	VSS011
15	VSS020
16	TAB

CBTL02043ABQ_QSD

Pin	Function
1	+MUX_PWR
2	VDD001
3	

USB3_TXN3_B0+ C229 USB3_TXP3_B0+ C USB3_TXN3_B0- R168 shortTYP_C@0.4 USB3_TXN3_B0+ USB3_RXP3_B1+ R514 shortTYP_C@0.4 USB3_RXN3_B1- R520 shortTYP_C@0.4 USB3_TXP3_C0+ C214 USB3_TXN3_C0- C USB3_RXP3_C1+ R153 shortTYP_C@0.4 USB3_RXN3_C1- R207 USB3_TXN3_C0- R147 shortTYP_C@0.4 USB3_RXP3_C1+ R511 shortTYP_C@0.4 USB3_RXN3_C1- R494 shortTYP_C@0.4 USB3_RXN3_C1-

[illegible][illegible]

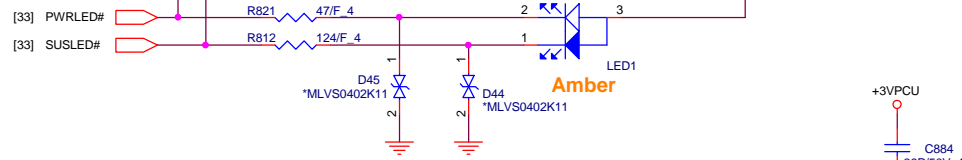
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

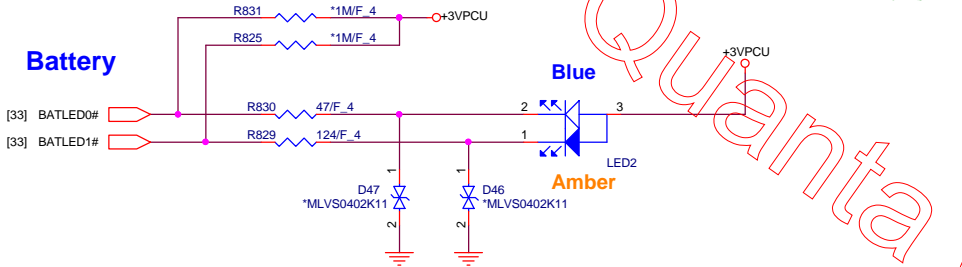
Quanta P/NAMAZING P/NUSD**保護位置**
BC104308Z00, AZ1043-08F.R7G0.08TX RX (USB3.0 GEN1 5G)
BC104508Z00, AZ1045-08F.R7G0.08D+ D- SBU1 SBU2 CC1 CC2
BC005725Z00, AZ5725-01F.R7G0.009 PD 5V (follow ZAA)

LED(UIF)

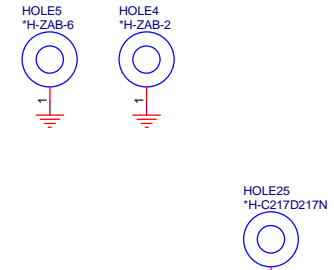
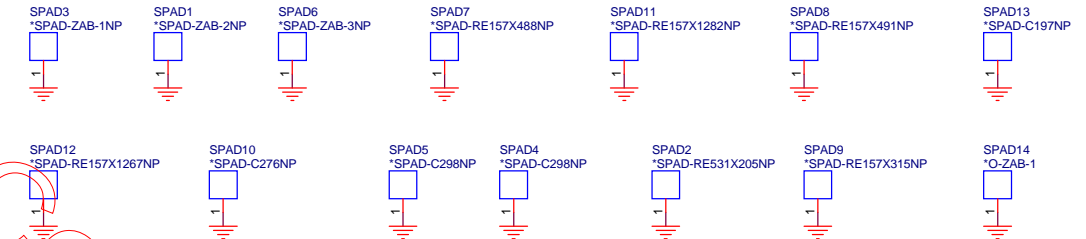
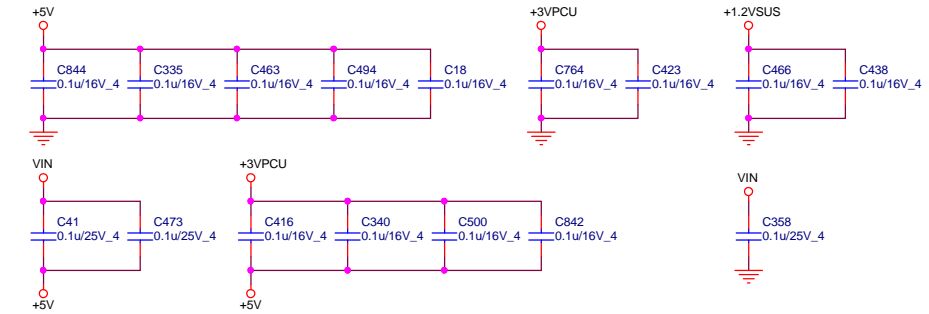
Power LED



Battery

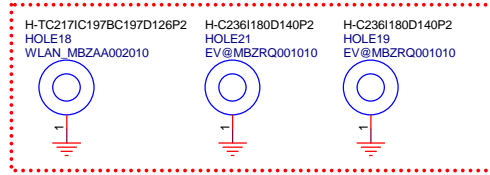


Stich cap

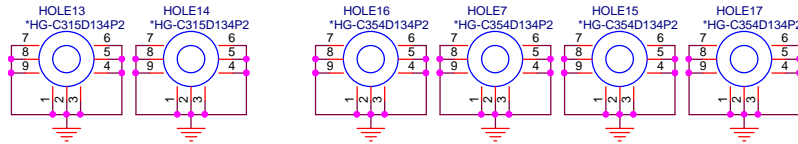
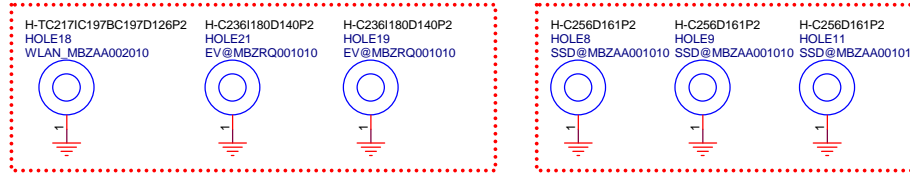



HOLE(OTH)

Layout set on Bottom

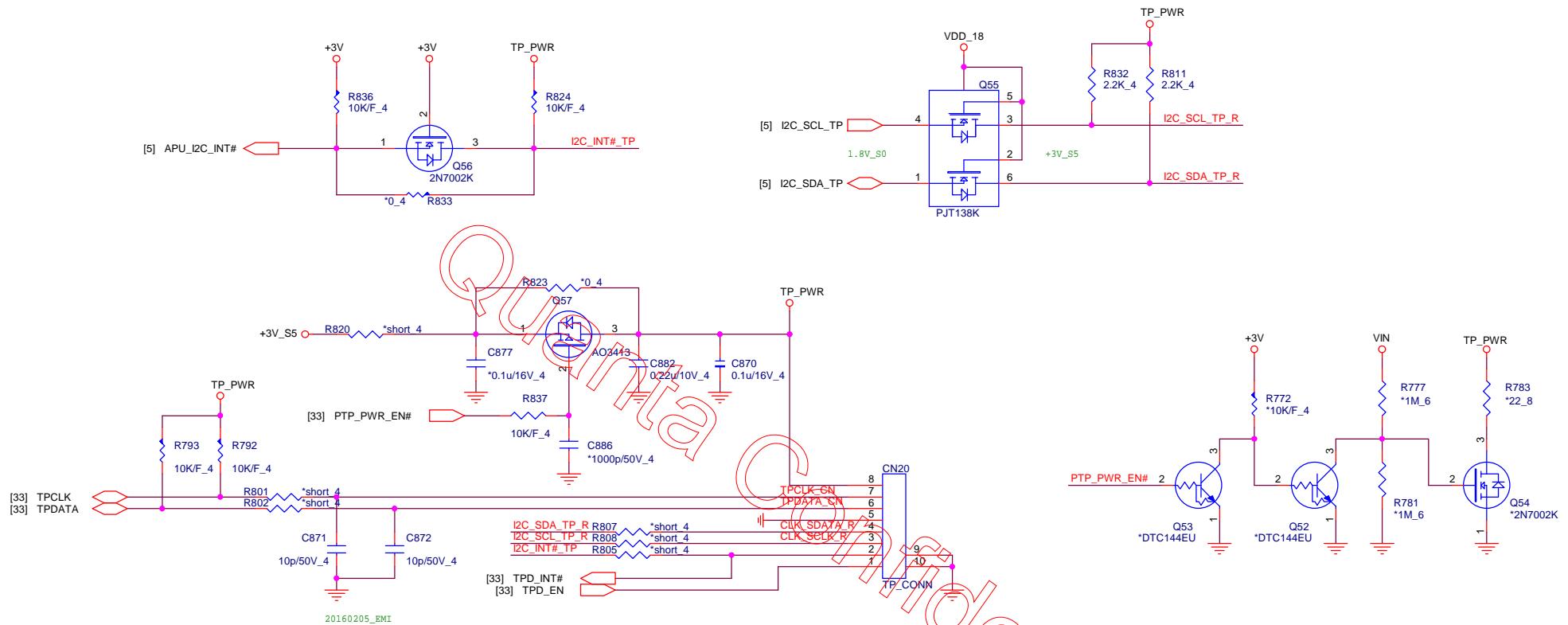


Layout set on BOT

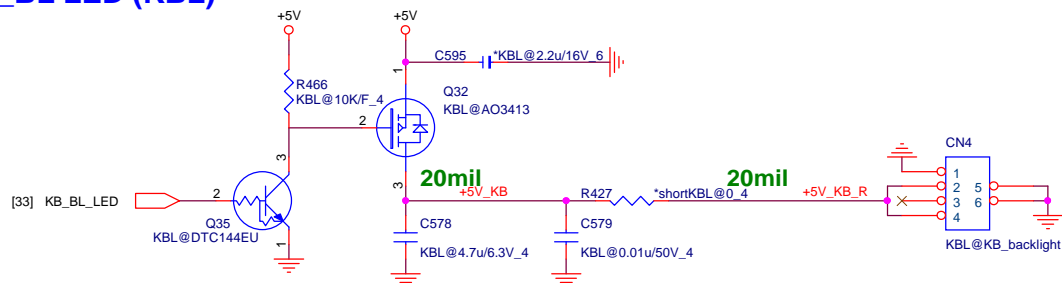
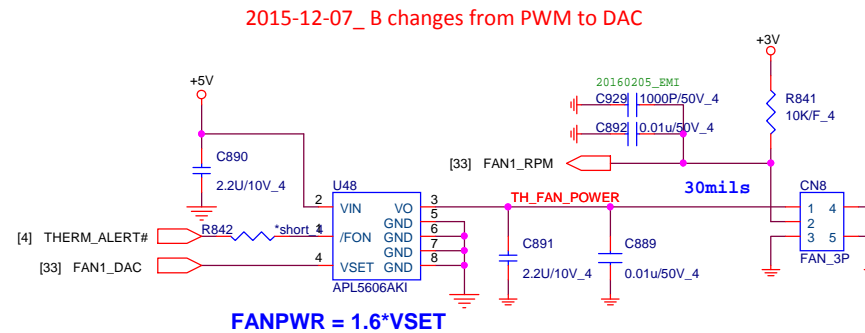


 Quanta Computer Inc. PROJECT : ZAB	
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LED/HOLE/EMI	
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TOUCH PAD(TPD)



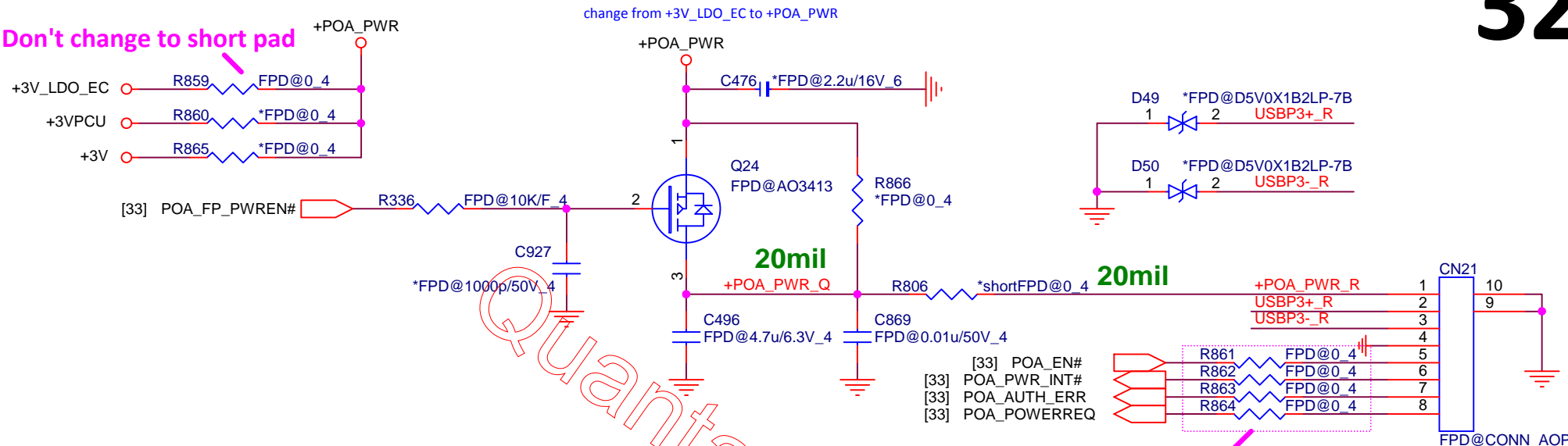
31



POA(FPD) or PBA

32

Don't change to short pad



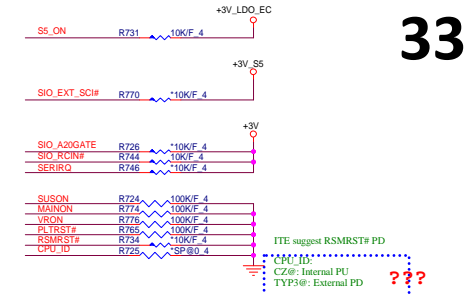
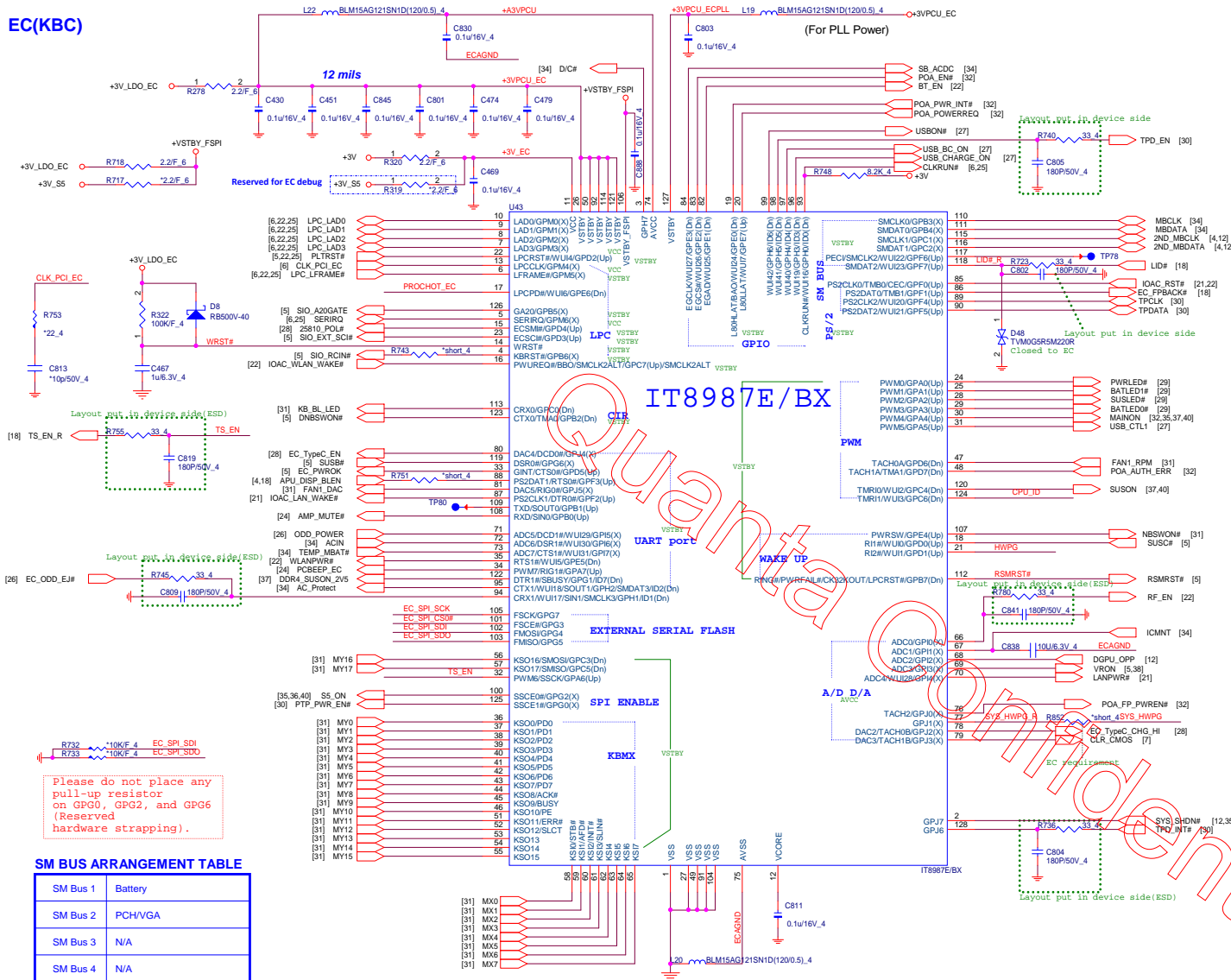
SEL	OE#	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

Spec define: High Active

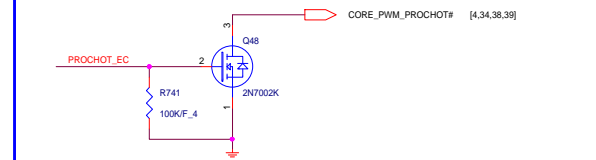
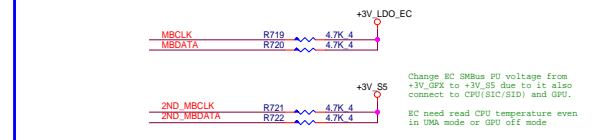
Quanta Computer Inc.

PROJECT : ZAB

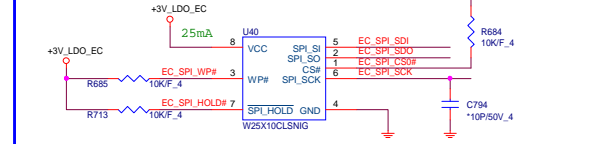
Size	Document Number	Rev
	POA	1A
Date:	Friday, March 04, 2016	Sheet 32 of 45



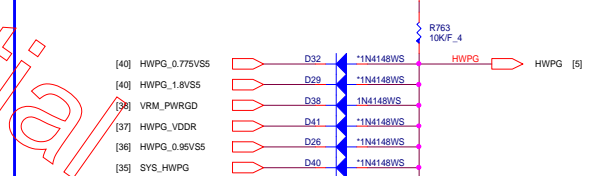
SM BUS PU(KBC)



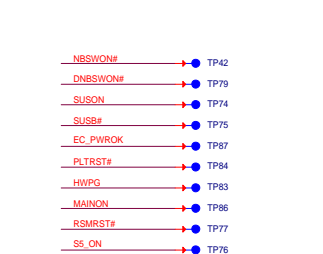
SPI NOR FLASH(128KB) (KBC)



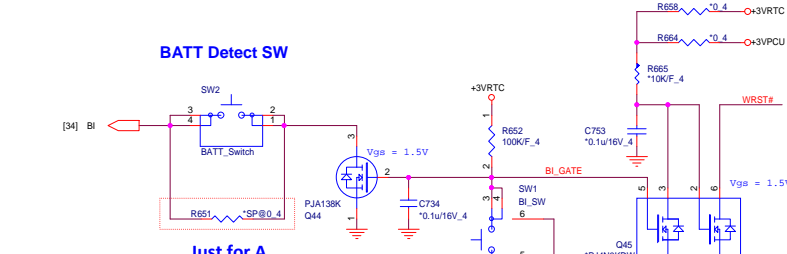
HWP(KBC)



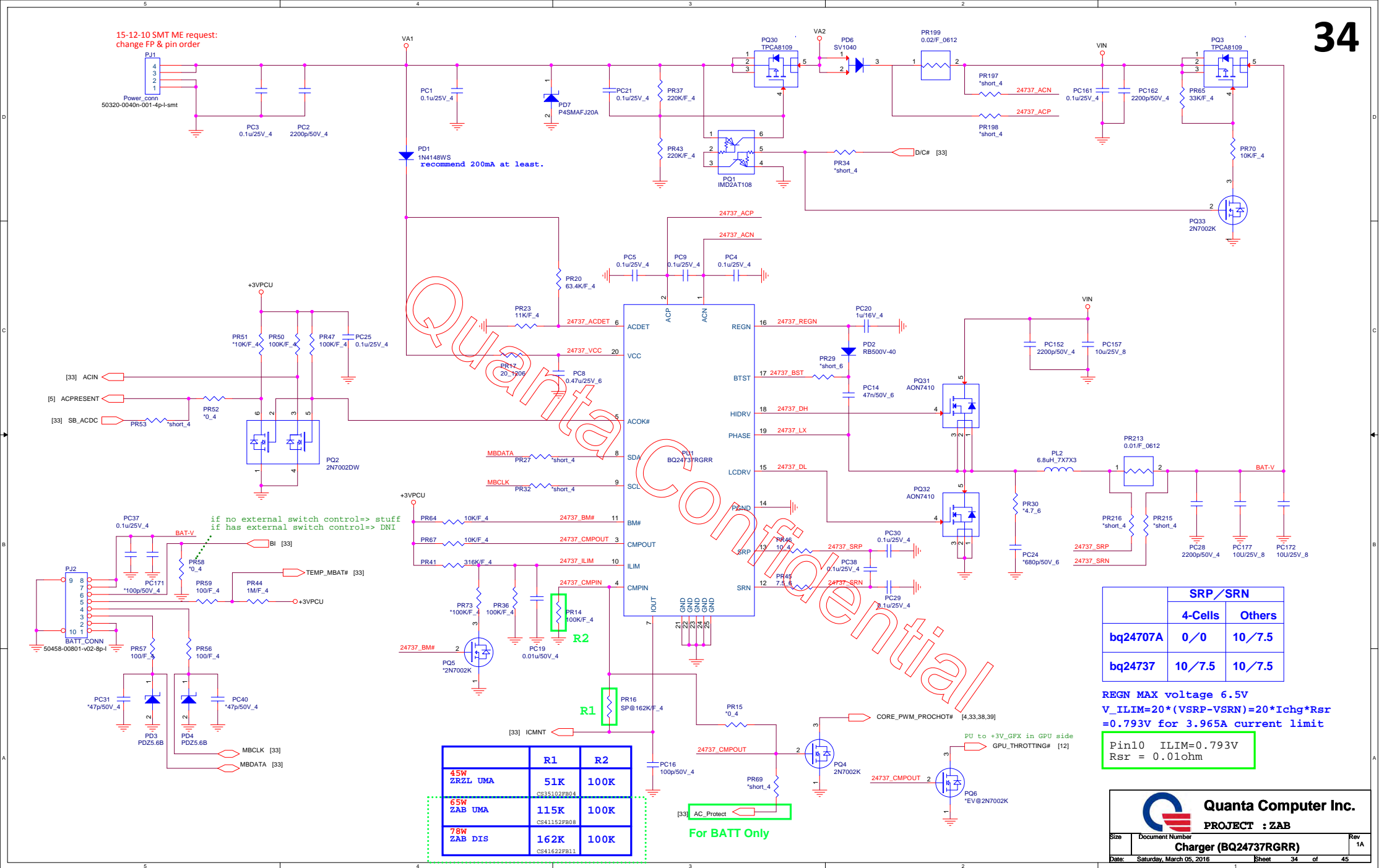
Power sequence

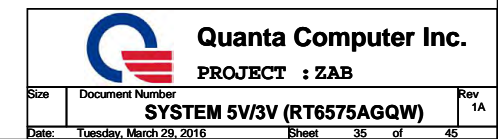


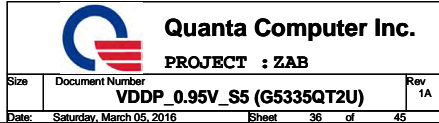
Battery B/I SW (SYP)

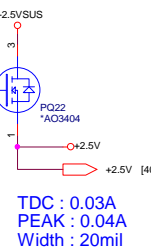
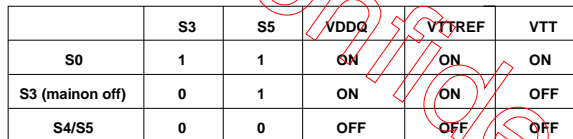


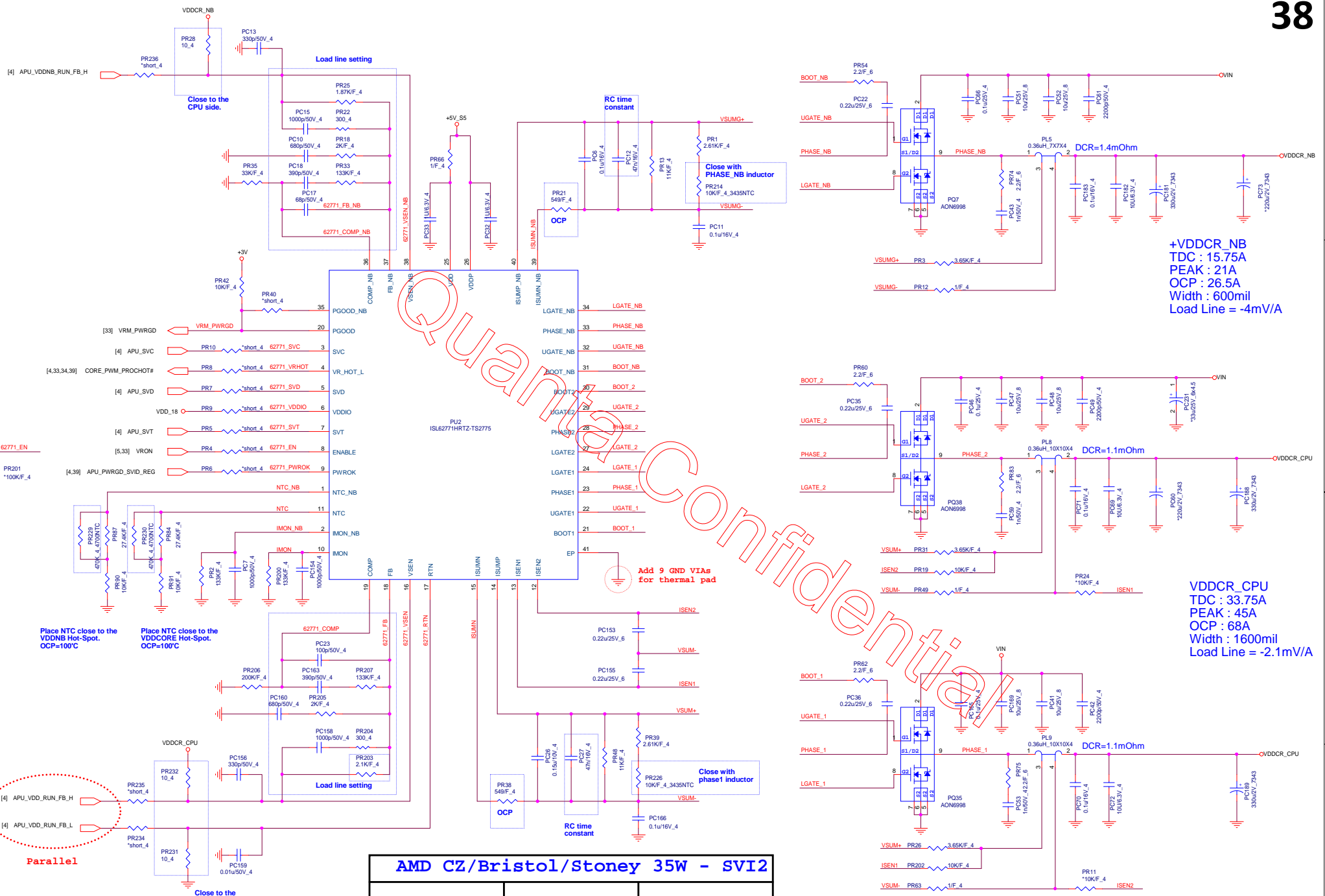
15-12-10 SMT ME request:
change FP & pin order



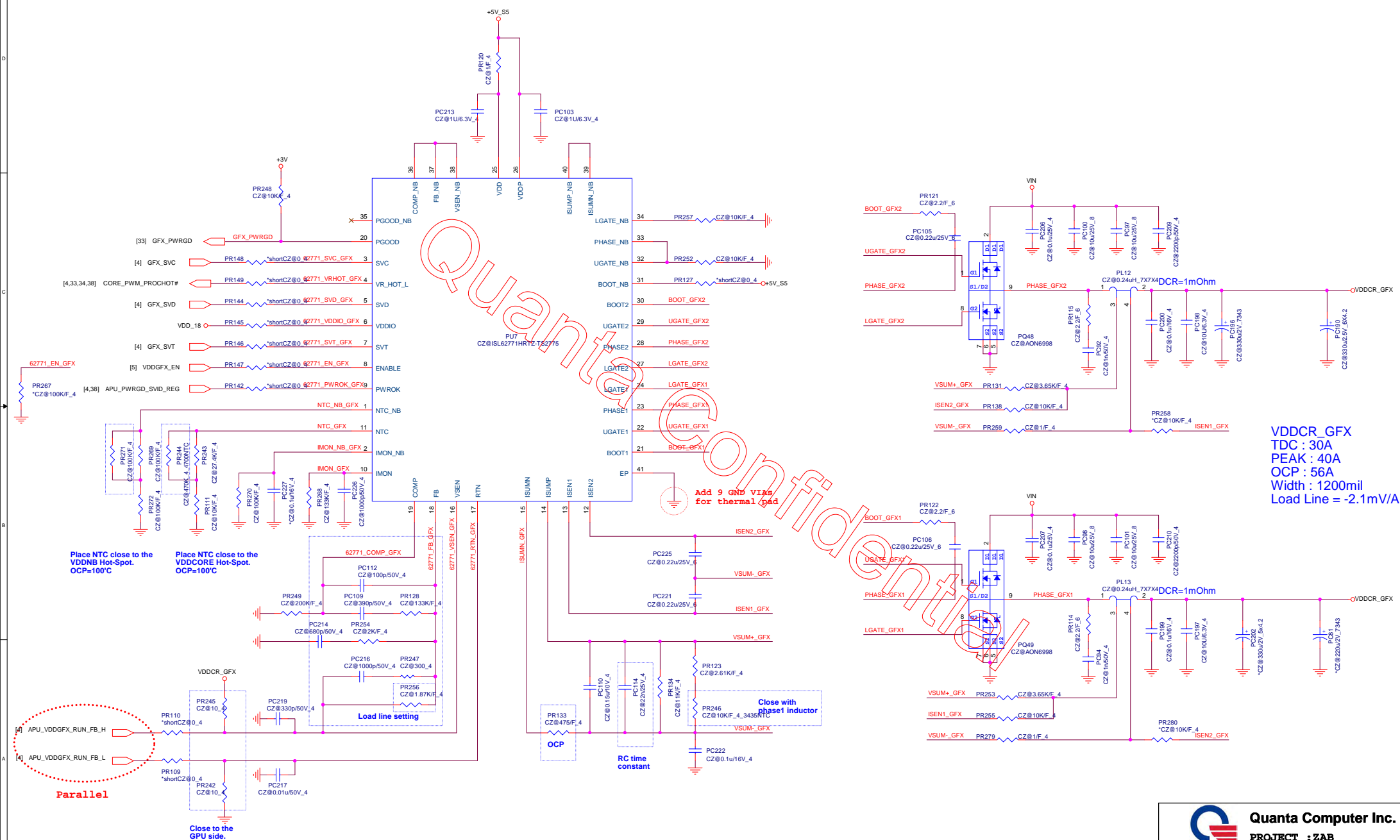


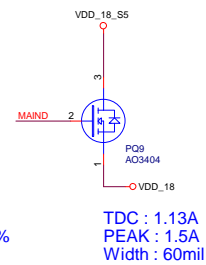
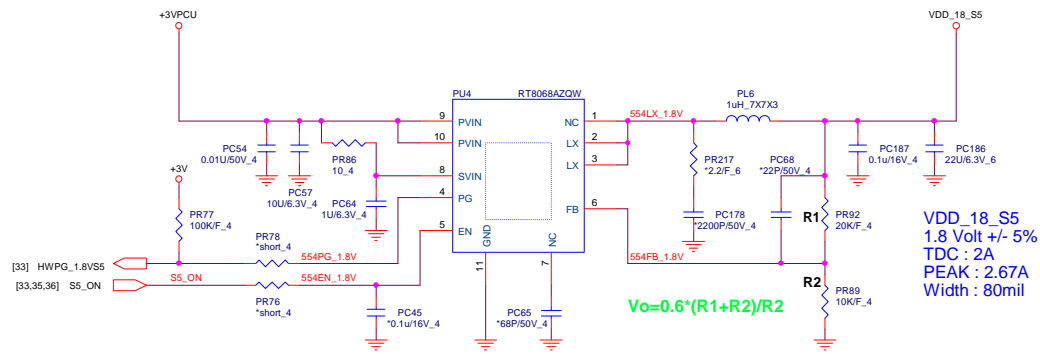






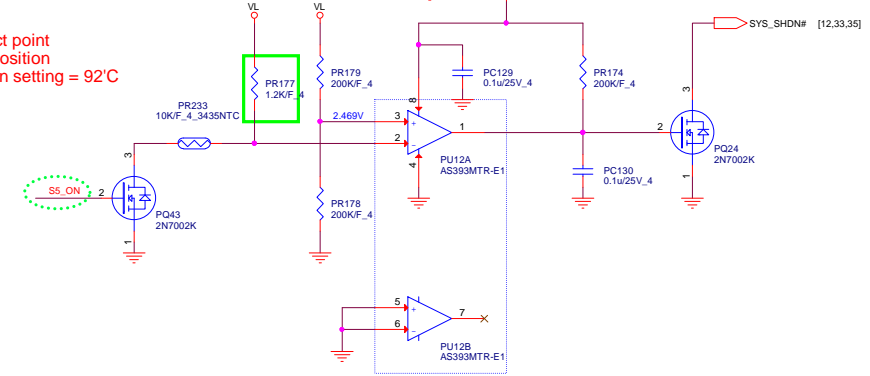
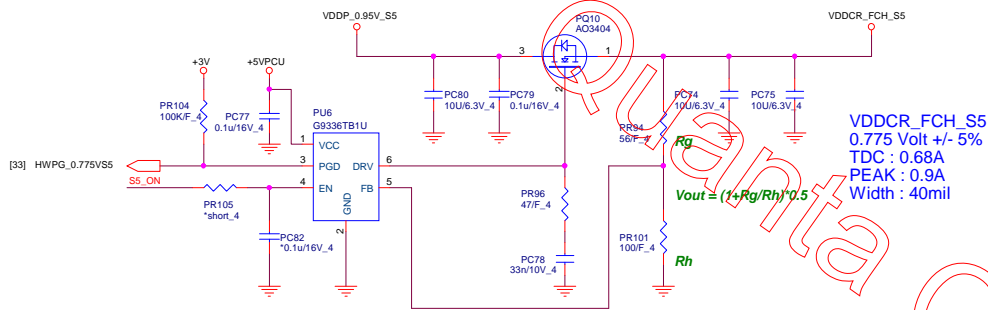
AMD CZ/Bristol/Stoney 35W - SVI2		
+VDDCR_NB TDC : 15.75A PEAK : 21A OCP : 26.5A Width : 600mil Load Line = -4mV/A	+VDDCR_CPU TDC : 33.75A PEAK : 45A OCP : 68A Width : 1600mil Load Line = -2.1mV/A	+VDDCR_GFX TDC : 30A PEAK : 40A OCP : 56A Width : 1200mil Load Line = -2.1mV/A



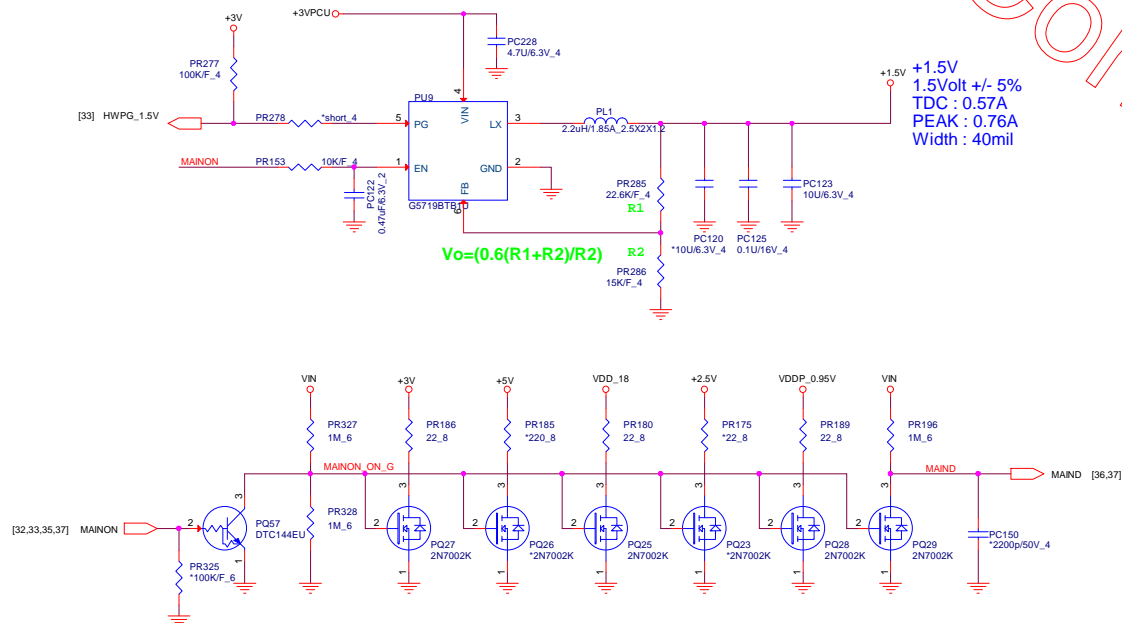
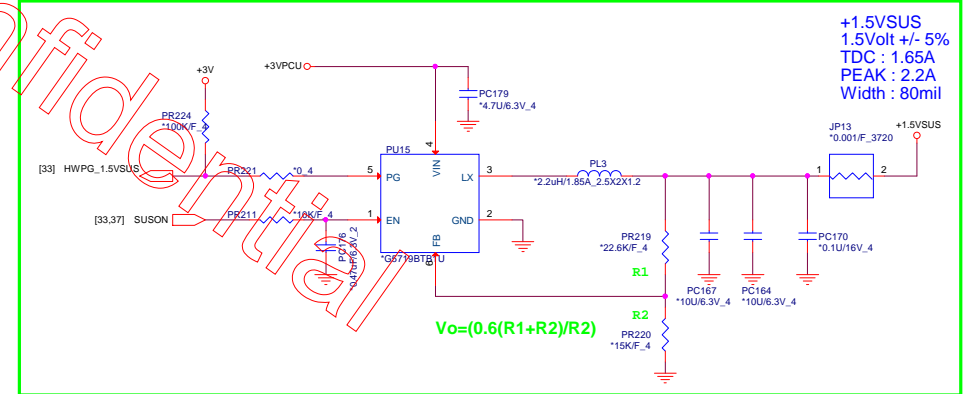


Thermal Protection

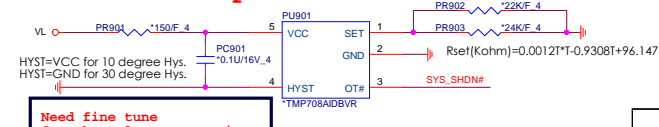
- (1) Need fine tune for thermal protect point
- (2) Note placement position
- (3) Thermal protection setting = 92°C



+1.5VSUS Reserve for +1.5V Wifi Card



Thermal protection



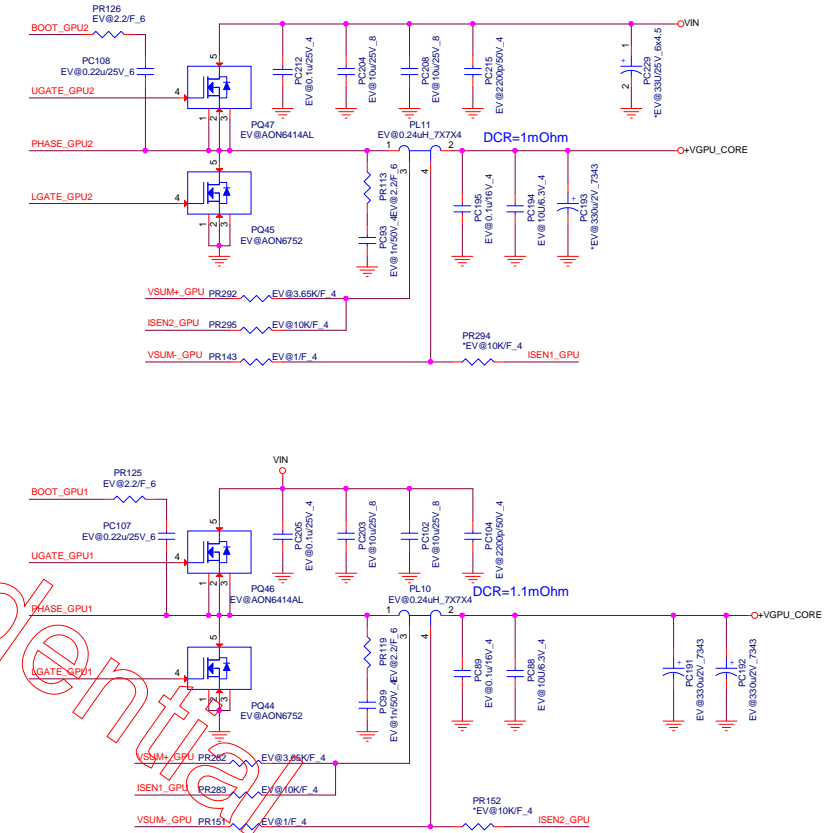
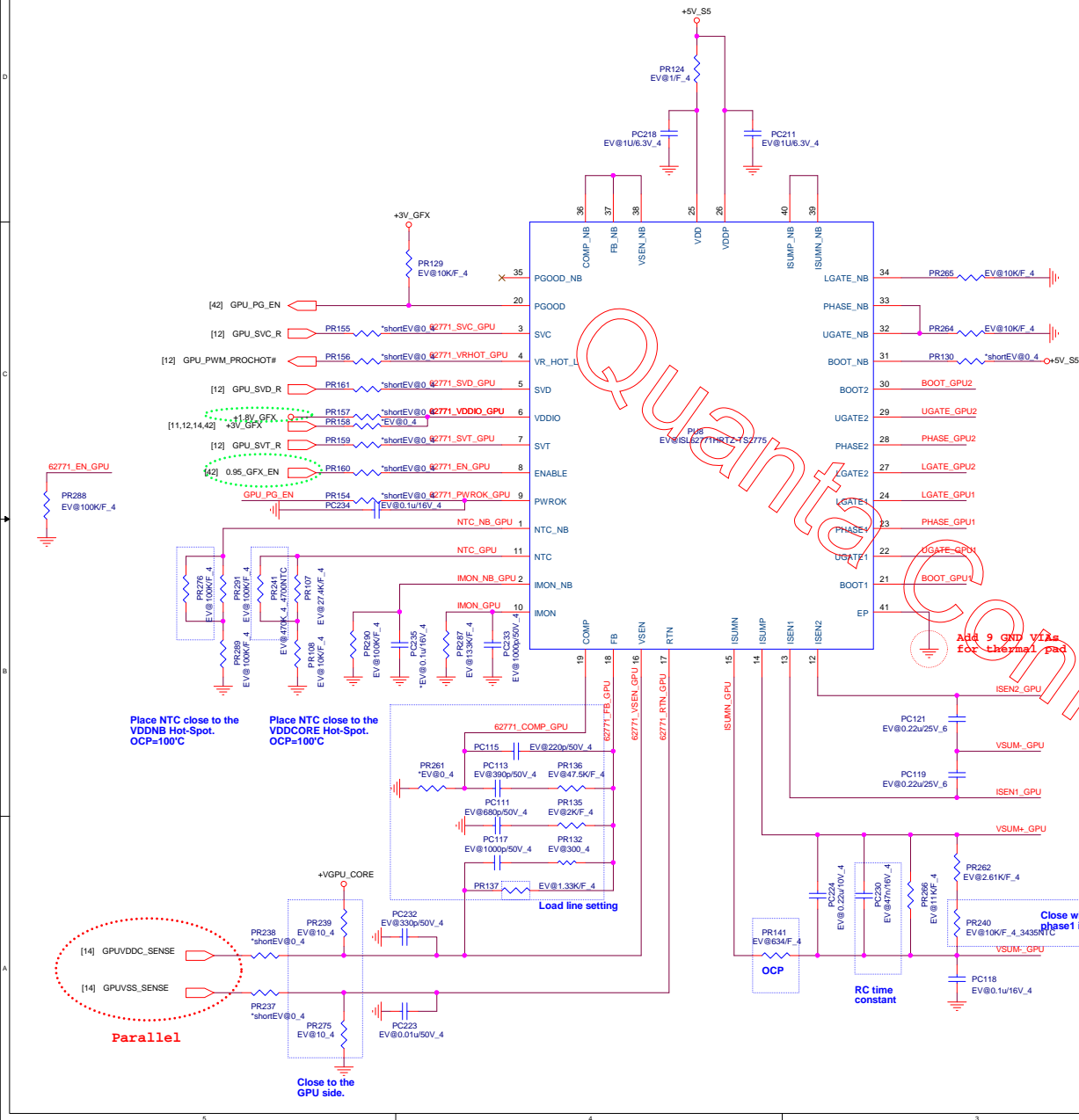
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PROJECT : ZAB

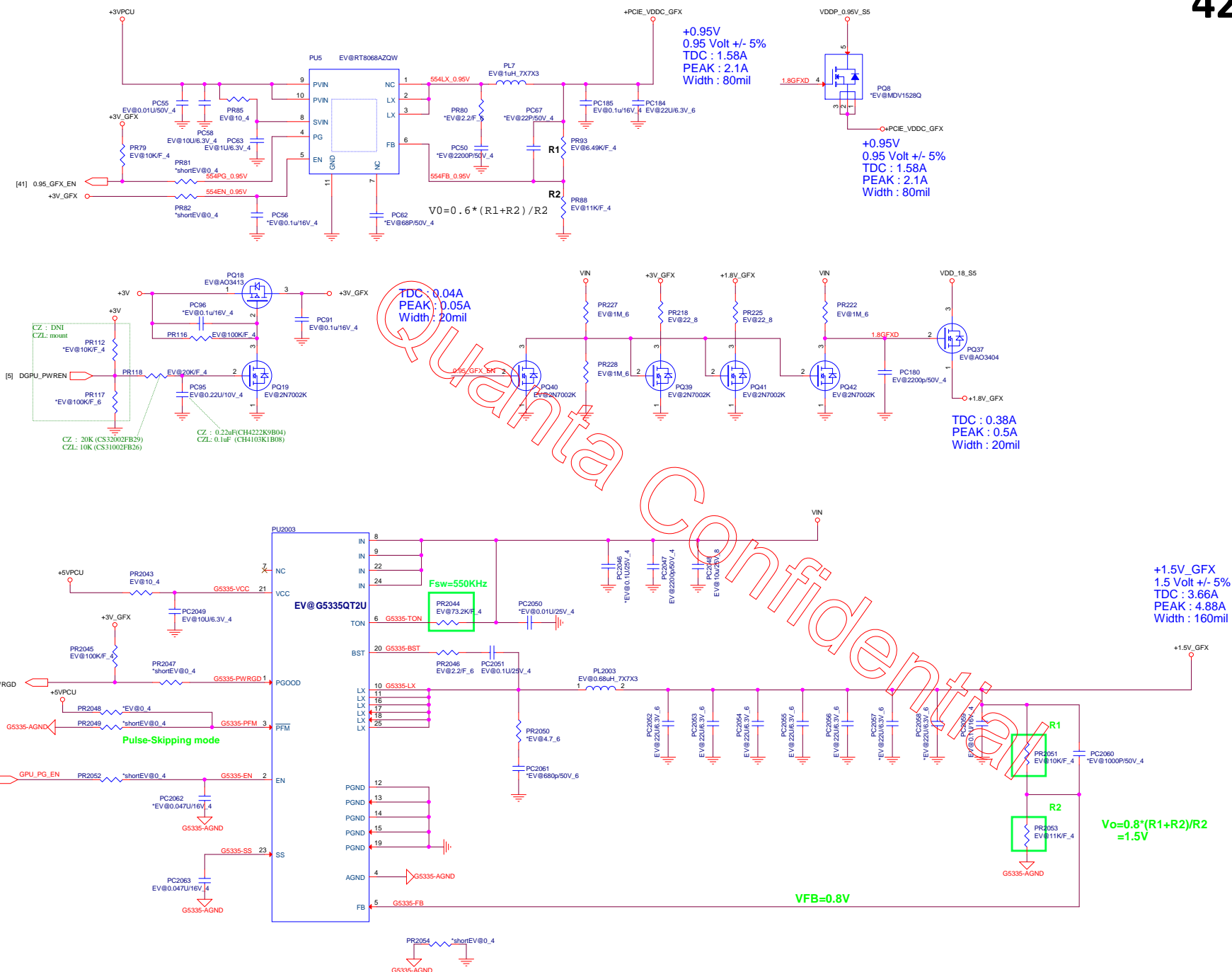
Size	Document Number	Rev
	+1.8V/+0.775V/+1.5V/Thermal	1A
Date:	Friday, March 18, 2016	Sheet 40 of 45

Interface SVI2

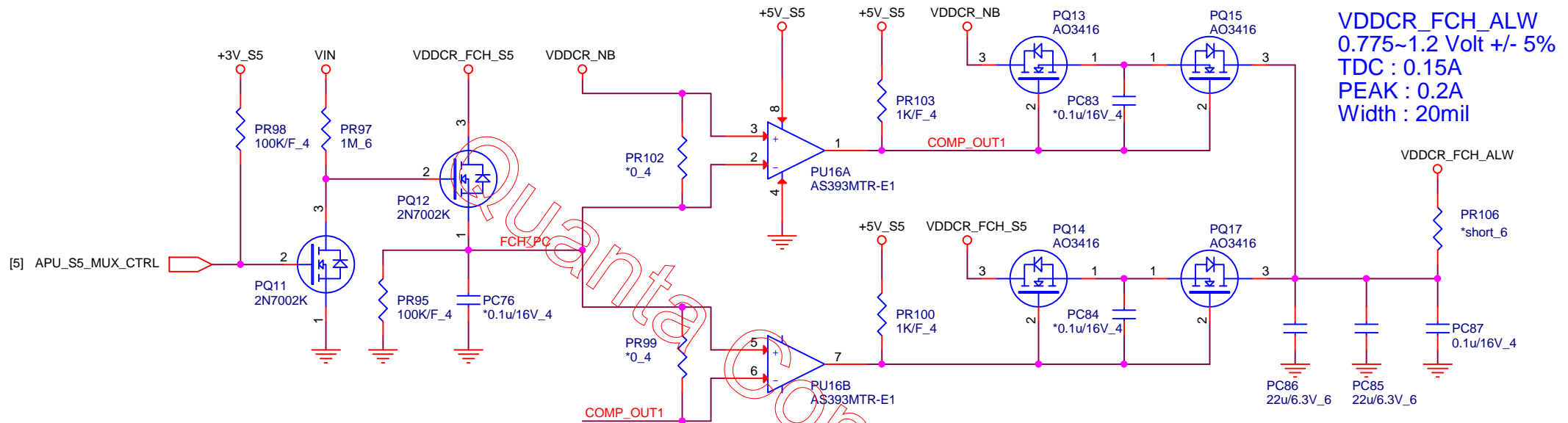
R16M-M2-50 (37W)

TDC : 45A
PEAK : 60A
OCP : 75A
Width : 1600mil
Load Line = -1mV/A





For Type 1 & 3



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Size	Document Number	Rev
	VDDCR_FCH_ALW	1A

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MODEL	REV	Change List	Model	ZAB M/B	
			Page	From	To
ZAB M/B	A	2015-11-03 Change DP to VGA IC from IT6516 to RTD2166 (cost) First Release	1		
			2		
			3		
			4		
	B	2015-xx-xx Add	5		
			6		
			7		
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Power Rail	Description	Range	S0	S3	S5
VDDCR_CPU	APU power	0.75~1.5	ON	OFF	OFF
VDDCR_NB	APU NB power	0.75~1.2	ON	OFF	OFF
VDDCR_GFX	APU GFX power	0.75~1.2	ON	OFF	OFF
VDDCR_FCH_S5	APU FCH core logic power	0.775~1.2	ON	ON	ON
+SMDDR_VREF	DDR power	0.6	ON	ON	OFF
+SMDDR_VTT	DDR power	0.6	ON	OFF	OFF
+1.2VSUS	APU & DDR power	1.2	ON	ON	OFF
+2.5V	DDR power	2.5	ON	OFF	OFF
+1.5V	1.5V power rail	1.5	ON	OFF	OFF
+1.5VSUS	1.5V switched power rail	1.5	ON	ON	OFF
VDDP_0.95V	0.95V switched power rail	0.95	ON	OFF	OFF
VDDP_0.95V_S5	APU power	0.95	ON	ON	ON
VDD_18	1.8V switched power rail	1.8	ON	OFF	OFF
VDD_18_S5	1.8V power rail	1.8	ON	ON	ON
+3V	3.3V switched power rail	3.3	ON	OFF	OFF
+3V_S5	3.3V power rail	3.3	ON	ON	ON
+3VPCU	3.3V always	3.3	ON	ON	ON
+5V	5V switched power rail	5	ON	OFF	OFF
+5V_S5	5V power rail	5	ON	ON	ON
+5VPCU	5V always	5	ON	ON	ON
+VGPU_CORE	GPU power	0.8~1.225	ON	OFF	OFF
+1.5V_GFX	GPU power	1.5	ON	OFF	OFF
+PCIE_VDDC_GFX	GPU power	0.95	ON	OFF	OFF
+1.8V_GFX	GPU power	1.8	ON	OFF	OFF
+3V_GFX	GPU power	3.3	ON	OFF	OFF
VIN	Adaptor power supply	11.1~19	ON	ON	ON



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	POWER STATUS	1A
Date:	Friday, January 29, 2016	Sheet 45 of 45